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An Improved Reliability Model for NMR

by

D. P. Siewiorek

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Technical Report No. 24

This work was supported by the
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DIGITAL SYSTEMS LABORATORY

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ABSTRACT

The classical reliability model for N-modular redundancy (NMR) assumes the network to be failed when a majority of modules which drive the same voter fail. It has long been known that this model is pessimistic since there are instances, termed compensating module failures, where a majority of the modules fail but the network is nonfailed. A different module reliability model based on lead reliability is proposed which has the classical NMR reliability model as a special case. It is shown that the standard procedure for altering the classical model to take compensating module failures into account may predict a network reliability which is too low in some cases and too high in others. It is also demonstrated that the improved model can increase the predicted mission time (the time the system is to operate at or above a given reliability) by 50% over the classical model prediction for a simple network.

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INTRODUCTION

New system designs for reliable computers must be explored to meet the increasing demand for reliable computing systems. In order to select one design approach over another a method of comparison must exist. One important method of comparison is the modeling of the system reliability.

Modeling requires a mathematical or physical representation which incorporates the salient parameters of the modeled system [1]. A model is an incomplete representation of the subject under study. To be of value, the modeling technique must be convenient to apply and must successfully predict the behavior of the subject under various parameter changes. If a reliability model is accurate, then insights can be gained as to how the system reliability changes as a function of the design parameters.

A modification to the classical reliability model for N-modular redundancy (NMR) is presented and demonstrated to increase the predicted mission time (the time the system is to operate at or above a given reliability) by 50% for a simple network.

THE PROBLEM

NMR [2] is implemented by dividing the nonredundant network into modules, replicating the modules N times (where N = 2t + 1 and t is an integer), and inserting a majority gate between each set of replicated modules. Figure 1 depicts the implementation of a triple modular redundancy (TMR) version of a multiple input, single output, nonredundant module. TMR will be the major topic of discussion, although the procedures presented have straightforward applications to the general case of NMR.

Classically the reliability of the network in Fig. 1 is modeled by assigning the modules a reliability function, call it $R_m(t)$, or R_m with time as an understood variable. The probability of module failure is thus $1 - R_m$. It is then assumed that the system fails when two or more modules driving the same voter fail. For example, under this assumption there are four cases of module failures for which the network of Fig. 1 does not fail: 1) no module failures, 2) only module one fails, 3) only module two fails, and 4) only module three fails. Summing over all four nonfailure situations yields the following reliability model:

$$R_m^3 + 3R_m^2(1 - R_m) \tag{1}$$

However, even though a module fails, the function it realizes at its output may be very different from the function realized by some other failed module. Thus a majority of modules could fail but the system not fail since at any given instant of time the majority of

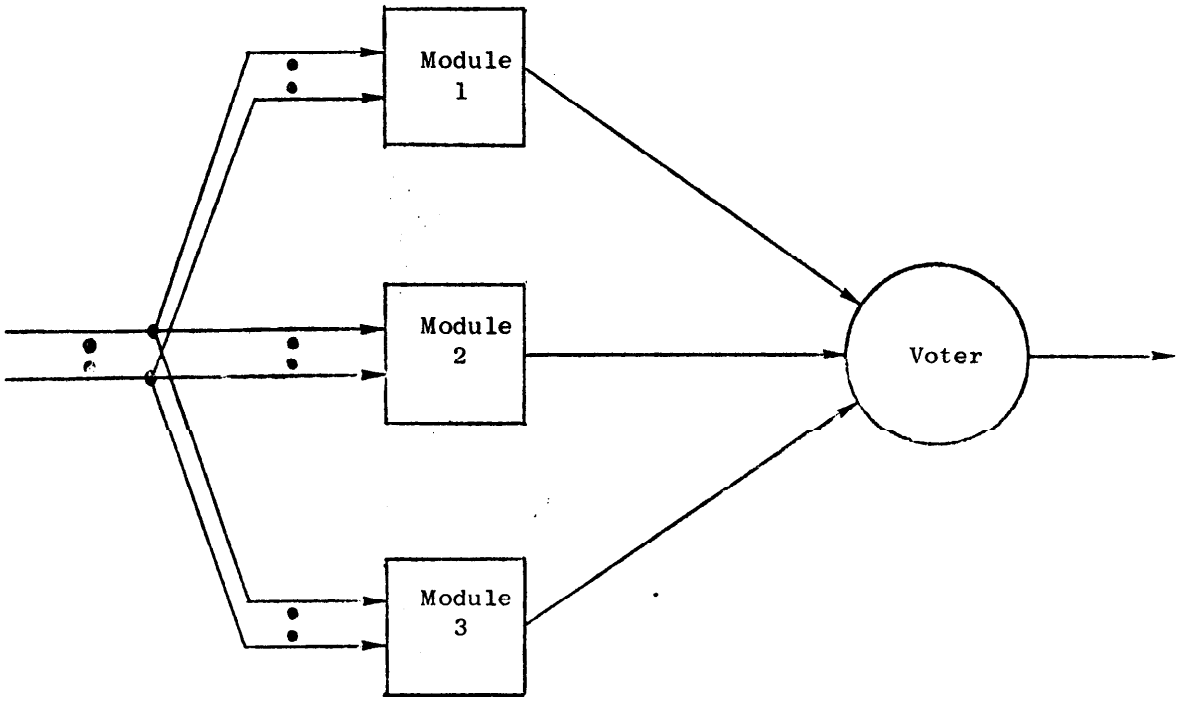


Fig. 1. Classical triple-modular redundancy

module outputs are in the correct state. And, in fact, there are a substantial number of cases for any given module such that the network could still realize its designed function even though two or more modules in a trio, such as Fig, 1, are considered failed under the assumptions of the classical reliability model. For example, consider two failed modules for the network of Fig. 1. Assume module one has a permanent logical one on its output while module three has a permanent logical zero output. The network will still realize its designed function since the nonfailed module, module two, (whose output can take on one of two states, logical one or logical zero) and one of the two failed modules will always be in agreement for a given instant of time. The voter will thus always see a majority of inputs with the correct value. Such multiple module failures which do not lead to network failures will be termed compensating module failures.

Adding these double, and even triple, module failure cases can often lead to a substantially higher predicted reliability for the same network than for the classical reliability model. With a better reliability model some systems previously designed may be found to be overdesigned for their specific mission because an inadequate reliability model was used. Both in the realm of aerospace, where weight and power consumption are critical quantities, and the commercial world, where the dollar is king, such overdesigns are to be avoided.

Module Failure Model

Research in the area of testing and diagnosing combinational and sequential logic circuitry has relied heavily on the logical stuck-at-fault model [3]. This model assumes that most or all

failures of interest in a logic circuit manifest themselves as some line in the circuit taking on a constant logical value, either one or zero. Now that algebraic structure which applies to the behavior of networks in the presence of stuck-at faults has been developed [3], the tools are available to formulate and analyze a new module reliability model.

The new model will assign a reliability function to each lead in the network rather than each module as in the classical model. Lead reliability will be represented by R and the probability of lead failure by 1 - R.

Much has been written in defense of the stuck-at failure model [3] but a few words will now be devoted to justification of the lead reliability model. In one study of IC failure mechanisms [4] it was found that about 50% of the IC failures were directly related to lead failures, either input leads or metalization on the chip itself. A more recent study also developed a 50% [5] figure while yet another survey [6] indicated that 84% of the IC chip failures were directly related to some form of lead failure. What remaining proportion of the failures could be modeled as lead failures is an area for further research.

Similar to the classical model assumption that module failures are statistically independent events, it will also be assumed that lead failures are statistically independent. If the major source of IC failures after the production line testing and initial burn-in period are associated with package leads or chip metalization, or can be modeled as lead failures, then this model is very appropriate. However, data on IC failure mechanisms and their logical effect is

difficult to find in the open literature and this is an area for future research. Once the failure mechanisms are understood, failure and reliability models can be developed. A further advantage of the lead reliability model is that it takes into account the increased number of interconnections required for the massive redundancy version of a nonredundant system. Wiring errors and off-chip interconnections then may be the major source of failures.

The reliability model will now be formally presented. Figure 2 shows circuit schematics for a DTL and TTL gate. The block diagram divides a logic gate into a common part and branch input parts. The portions of the DTL and TTL gates to the left of the dotted line represents the branch parts of the gates, that to the right the common part. This is similar to the gate model used by Jensen [7]. If lead failure is the primary failure mechanism (through bounding or solder failures), the branch and common parts could be assumed to be perfectly reliable. If not, the branch part reliability (such as a diode failure in the DTL gate) would also be a factor in R. Furthermore, the common part reliability would be a factor in all the reliabilities of the leads the gate feeds.

One further assumption will be made. It will be assumed that the reliability of a lead can be represented as a sum of the reliabilities that the lead is not failed in a logical stuck-at-one (s-a-l) mode and that the lead is not failed in a logical stuck-at-zero (s-a-0) mode; i.e.,

$$R_{lead} = R_{s\text{-}a\text{-}l} + R_{s\text{-}a\text{-}0}$$

This model is not totally without precedence in the literature.

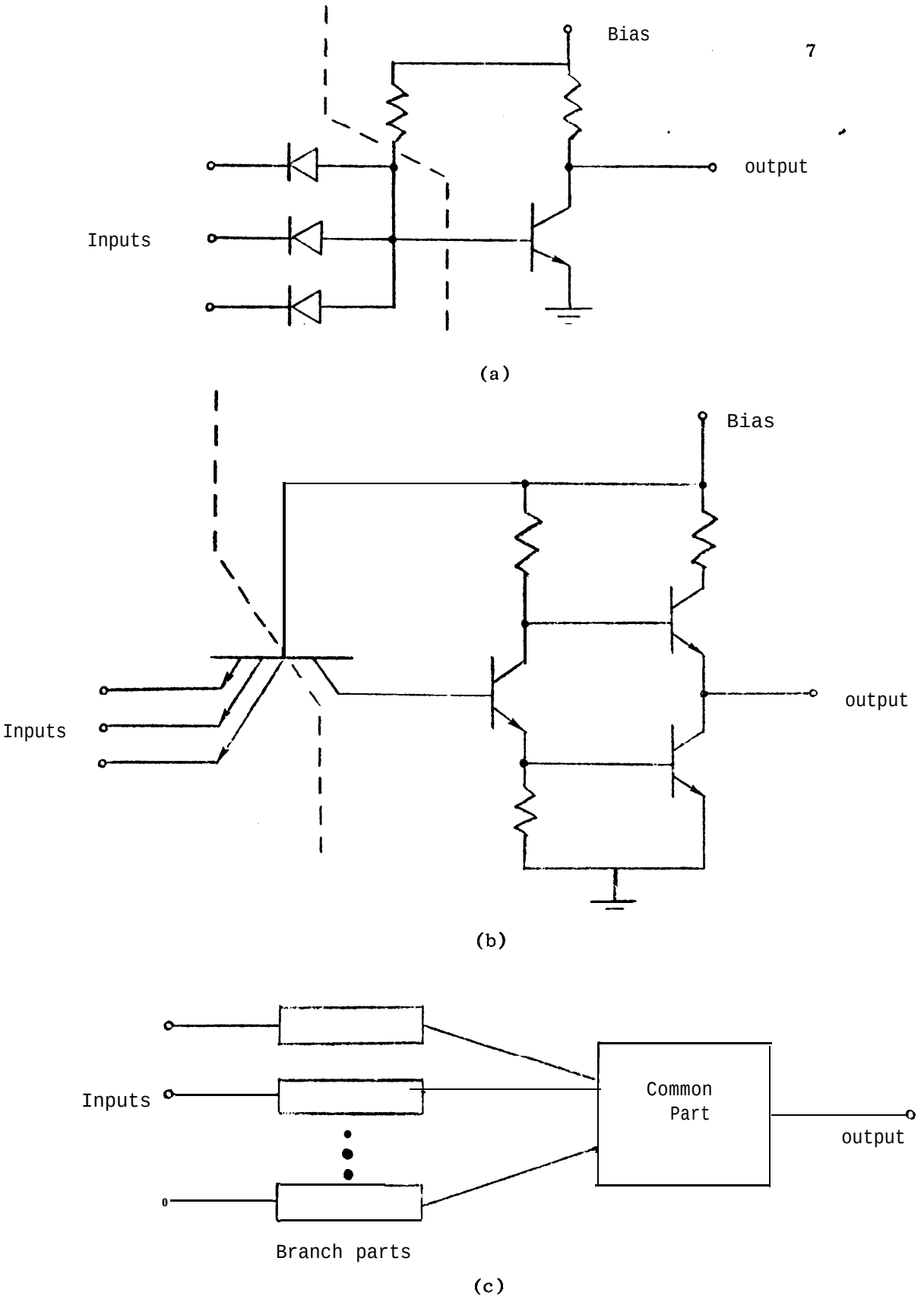


Fig. 2. DTL (a) and TTL (b) logic gates and their model (c).

Klaschka [8] calculates gate reliabilities as a function of the gate common parts open or short circuiting. The gate reliability used by Jensen [7] is a function of gate common parts stuck-at zero or one, depending on whether the output transistor shorts or opens and the logical representation of these failures in the logic technology used, as well as branch part failures.

So as not to unnecessarily complicate the following formulation, it will be further assumed that s-a-l and s-a-0 faults are equally likely. Thus:

$$R_{s\text{-}a\text{-}l} = R_{s\text{-}a\text{-}0} = R/2$$

In practice this may not be the case and the modifications necessary to the following algorithm will be obvious. In essence, $R_{s\text{-}a\text{-}l}$ and $R_{s\text{-}a\text{-}0}$ need only retain their separate identities.

Ascertaining the Effect of Compensating Module Failures on Reliability Modeling

Previous reliability models for TMR networks have assumed a module reliability R_m and have written the reliability of a simple serial cell such as Fig. 1 with perfect voters as:

$$R_{cell} = R_m^3 + 3R_m^2(1 - R_m)$$

Frequently (2) is rewritten to take into account the cases where two modules can fail so as to have compensating effects at the voter:

$$R_{cell} = R_m^3 + 3R_m^2(1 - R_m) + K(3\ R_m)\ (1 - R_m)^2 \qquad (3)$$

The K in (3) is a probability formed by the ratio of the number of ways in which, for a given cell, compensating failures can occur divided by the number of ways any failure can occur. In the literature [9] K has often been taken as 1/2. The value of K equal to 1/2 is commonly arrived at by assuming a failed module is just as likely to give an incorrect zero output as an incorrect one output. Of the four possible output combinations from two failed modules (00, 01, 11, 10) two, namely 01 and 10, are compensating module failures. Hence K = 2/4 = 1/2. That K = 1/2 doesn't hold for some typical module types is shown by example in the next section, Thus if K = 1/2 is used, (3) is no longer known to be a lower bound for cell reliability in the general case and simply becomes a "good guess". Without a careful analysis the choice of any K (except K = 0) casts doubts as to whether (3) is a lower or upper bound.

All faults will be assumed to be statistically independent permanent stuck-at-l (s-a-l) and stuck-at-0 (s-a-O) types [3]. Further, the modules are assumed to be irredundant so that any single internal module fault will cause an improper output for at least one set of inputs. Finally, it will be assumed that the cell has failed, and thus the system has failed, as soon as it is possible for the cell to give a wrong response to any possible input combination. This excludes the situations where a cell fails but subsequent faults within the cell restores the segment to proper behavior. For example, consider a module consisting of a single NOR gate. If one module had an output s-a-0 and another had an input s-a-l the voter would

always see two or more zeroes and produce a constant zero output. Now if the output of the second module became s-a-l (a second internal fault to that module) the voter would follow the healthy signal since the faulty modules cancel each other's effects. The system would now be functional.

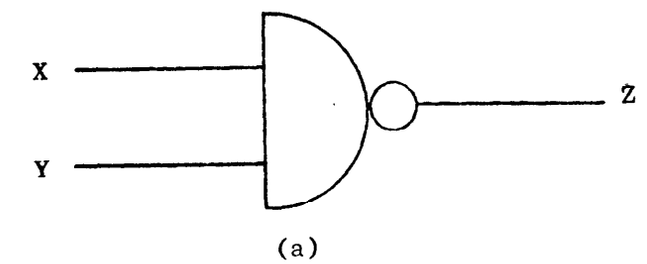
To model the faulty modules we will adopt the notation developed in [3]. We will now demonstrate the evaluation of the replacement for the third term of (3); i.e., the case of two faulty modules in a TMR cell.

1) Transform the logical circuit into the corresponding logical model [3].

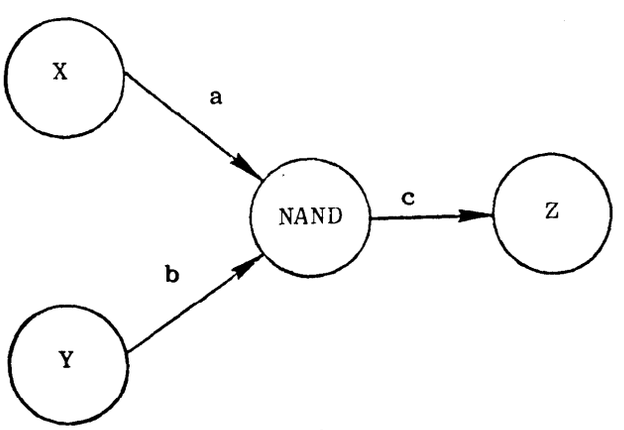
Consider Fig. 3 (a) where the module under study is a single two input NAND gate. The logical model is a directed graph shown in Fig. 3(b). It consists of a node for each network input and output in addition to a labelled node for each gate.

2) Form the functional equivalence classes for all single and multiple faults in the logical model [3].

A fault is said to be functional equivalent to another fault if and only if the output function realized by the network with only the first fault present is equal to the function realized when only the second fault is present. For example, the faults a/o (the notation ℓ/i means line ℓ stuck at logical value i) or c/l cause the NAND gate to yield a constant one output. Thus a/o and c/l are functionally equivalent. Table 1 shows the fault classes and their members. Here λ is the null fault and represents the fault free network. The functional equivalence classes are assigned numbers arbitrarily.



(a)



(b)

Fig. 3. An example module (a) for the calculation of supplementary classes and (b) its logical model.

There exist certain combinations of fault functions which, when processed by a majority gate, yield the same output function as the fault free network. These combinations will be called supplementary classes and their formulation will be illustrated under the next step of the algorithm.

3) Enumerate the supplementary classes.

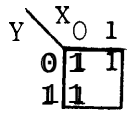
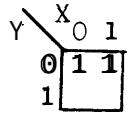
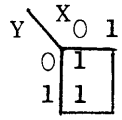
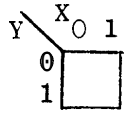
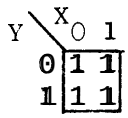
We will evaluate the replacement for the third term in (3); i.e., the case of two faulty modules in a TMR cell.

Thus each supplementary class will contain three members, one of which will be the fault free function. The majority gate can be considered to be a threshold gate with input weights 1 and threshold of 2 [10].

In Table l(b) the Karnaugh maps represent the fault functions for the faults λ, a/l, and b/l respectively. The threshold map is formed by summing the number of ones in each square of the Karnaugh map (fundamental product) over all three maps. After applying the threshold value of two we get the voter output function. We continue to try all possible combinations of faulty function pairs until all supplementary classes are formed. These are shown in Table 3(c) for our example; the fault free function λ (number 1) is implicitly a member of each supplementary class when two out of three (4) modules are faulty.

In the last step a matrix E is used to actually evaluate the replacement for the third term in (3). Element $E_{i,j}$ of equivalence class matrix E is the number of faults in equivalence class j (the equivalence classes were assigned numbers under step 2) which are a result of i leads in a module failing, where i is termed the fault multiplicity.

Table 1. The (a) fault classes, (b) an example of the test for supplementary fault classes, and (c) the supplementary classes for the NAND gate example of Fig, 3.

Class	Fault Function	Maps
$C_{F1} = \{\lambda\}$	$\bar{X} + \bar{Y}$	
$C_{F2} = \{a/1\}$	$\bar{Y}$	
$C_{F3} = \{b/1\}$	$\bar{X}$	
$C_{F4} = (c/0;$ $a/1, c/0; a/0, c/0; a/1, b/1;$ $b/1, c/0; b/0, c/0;$ $a/1, b/1, c/0; a/1, b/0, c/0;$ $a/0, b/0, c/0; a/0, b/1, c/0\}$	0	
$C_{F5} = \{a/0; b/0; c/1;$ $a/1, c/1; a/0, c/1; b/1, c/1;$ $b/0, c/1; a/1, b/0;$ $a/0, b/0; a/0, b/1;$ $a/1, b/1, c/1; a/1, b/0, c/1;$ $a/0, b/0, c/1; a/0, b/1, c/1\}$		

(a)

#1 λ | #2 $a/1$ | #3 $b/1$ | Threshold Map | Voter output Function

(b)

$$\{ \begin{matrix} (2,3) & (2,5) & (3,5) & (4,5) \\ (3,2) & (5,2) & (5,3) & (5,4) \end{matrix} \}$$

(c)

4) Form the term for two faulty modules by use of the equivalence class matrix E and the equation:

$$R_{\substack{\text{Two failed}\\ \text{modules}}} = \binom{3}{2} \sum_{k=2}^{2p} \left(1/2^k \sum_{\ell=1}^{k-1} \left(E_{\ell,\, i} \cdot E_{k-\ell,\, j} \right) R^{3p-k} (1-R)^k \right. \quad \forall\ i,j \text{ such that } (i,j) \text{ is a supplementary class} \qquad (4)$$

where p is the number of leads in the module and k is the number of line failures in the two failed modules.

The development of step 4 is best given by an example. The equivalence class matrix for the NAND gate of Fig. 3 is derived from the entries in Table l(a) and is shown in Table 2.

There are 3 ways to pick 2 modules to be faulty from a trio which accounts for the factor of $\binom{3}{2}$ in (4). The inner sum is the total number of ways a total of k line failures in the two modules can still leave a cell working. Consider the supplementary class (4,5) for which $E_{1,4} = 1$ and $E_{1,5} = 3$. Hence there are $1 \cdot 3 = 3$ possible failures of the two faulty modules due to a total of two faults between the modules yielding the constant 0 function in the first module and the constant 1 function in the second which result in the NAND function after passage through a majority gate when the other module is working. If the lead reliability is R, the probability of a s-a-0 or a s-a-l is R/2. Since we only have two lead failures out of a total of $3 \cdot 3 = 9$ in the three modules, double faults from the supplementary class (4,5) adds a term of

$$\binom{3}{2} \cdot 1/2^2 \cdot 1 \cdot 3 \cdot R^{9-2} (1-R)^2$$

Table 2. The equivalence class matrix for the NAND gate of Fig. 3.

Number of Failed Leads	Equivalence Class 1	2	3	4	5
0	1	0	0	0	0
1	0	1	1	1	3
2	0	0	0	5	7
3	0	0	0	4	4

to the reliability. The parameter k is the total number of failed leads currently under consideration. For our example of two failed NAND modules (4) becomes:

$$\binom{3}{2}\left[(20/4)R^7(1-R)^2 + (72/8)R^6(1-R)^3 + (118/16)R^5(1-R)^4 + (96/32)R^4(1-R)^5 + (32/64)R^3(1-R)^6\right]$$

The analogous equation to (4) for a single module failure would be:

$$R_{\substack{\text{One failed}\\ \text{module}}} = \binom{3}{1} \sum_{k=}^{p} 1/2^k \cdot E_{k,\ i} \cdot R^{3p-k}(1-R)^k \qquad (5)$$

$\forall\ i$

The procedure outlined above is easily modifiable to handle the case of three module failures. The sum in (4) would have an upper bound on k of $3p$ and the inner sum would be a product of three equivalence class matrix entries:

$$R_{\substack{\text{Three failed}\\ \text{modules}}} = \sum_{k=3}^{3p}\left(1/2^k \sum_{\ell=2}^{k-1} \sum_{m=1}^{\ell-1} \left(E_{m,h} \cdot E_{\ell-m,\ i} \cdot E_{k-\ell,\ j}\right) \cdot R^{3p-k}(1-R)^k \right) \qquad (6)$$

$\forall\ h,i,j$ such that (h,i,j) is a supplementary class

Also, it is readily extendable to other multiple line redundancy techniques (NMR). In some instances R_{sa1} may not equal R_{sa0}. If such is the case, then the equivalence class matrix and equations (4,5,6) will become more complicated since the faults must retain some of their separate identities. One way to achieve this is to make

the entries, $E_{i,j}$, to the equivalence class matrix the probability of occurrence of fault multiplicity i in class j. $E_{i,j}$ would be the sum of the probabilities of the i multiplicity faults in equivalence class j. Equations (4,5,6) would become simpler, without factors in R, (l-R), and 2^{-k}. In some logic families one type of logical stuck-at fault may be much more likely than the other. If so, $R_{s\text{-}a\text{-}i}$ could be taken as approximately R and the fault equivalence classes formed by considering s-a-i type faults only. The comparison of this reliability model with the one of (2) and (3) will now be undertaken.

Comparison of Module Dependent and Module Independent Reliability Models

If there are p leads in a module, then the module reliability, $R_{m'}$ according to the module-dependent reliability model or fault equivalent model just presented is R^p. For the case of fewer than half the modules failing in an NMR network, the classical module-independent reliability model gives a cell reliability of:

$$R_{cell} = \sum_{i=0}^{\lfloor N/2 \rfloor} \binom{N}{i} R_m^{N-i} (1 - R_m)^i \qquad (7)$$

It will now be shown that the first $\lfloor N/2 \rfloor$ terms of the module dependent reliability model are identical to (7), the classical NMR reliability model.

Theorem: The module dependent reliability model proposed above has the same form as (7) for $\lfloor N/2 \rfloor$ or fewer module failures.

Proof: The probability of no module failures is $(R^p)^N = R_m^N$ which is the first term of (7). Now for any number of module failures less than or equal to $\lfloor N/2 \rfloor$, there is still a majority of working modules and any failure configuration of a failed module's lines would not

cause system failure. So to complete the proof of the theorem, all we need show is that the module-independent failure probability $(1-R_m)$ is equal to the module-dependent cell failure probability.

From (5) factoring out the term R^{2P} which is the reliability of two nonfailed modules and the $\binom{3}{1}_0$ term since the failed module has already been selected, the module-dependent failure probability becomes:

$$\sum_{k=1}^{p} 1/2^k \cdot E_{k,\,i\ \forall\ i} \cdot R^{p-k}(1-R)^k \tag{8}$$

The $E_{k,i}$ term, considering the cases for all i, is $2^k \binom{p}{k}_0$ since there are $\binom{p}{k}_0$ ways to select k failed leads from p. Each failed lead may be in one of two failure modes, s-a-1 or s-a-0, which accounts for the 2^k. Hence (8) becomes:

$$\sum_{k=1}^{p} \binom{p}{k}_0 (1-R)^k R^{p-k} \tag{9}$$

Adding and subtracting R^p from (9) yields:

$$-R^p + \binom{p}{0} R^p + \sum_{k=1}^{p} \binom{p}{k}_0 (1-R)^k R^{p-k} =$$

$$-R^p + \sum_{k=0}^{p} \binom{p}{k} (1-R)^k R^{p-k} \tag{10}$$

The binomial expansion formula is:

$$\sum_{r=0}^{m} \binom{m}{r} X^r \cdot C^{m-r} = (X+C)^m \tag{11}$$

Using (11) in (10) gives:

$$-R^p + \sum_{k=0}^{p} \binom{p}{k}_0 (1-R)^k R^{p-k} = -R^p + (R + 1 - R)^p$$

$$= -R^p + 1$$

$$= 1 - R_m$$

which is the probability of module failure using the module independent reliability model.

Q.E.D.

Equations (2) and (3) with $K = 1/2$ were plotted in Fig. 4 for a four level tree network consisting of 15 NAND gates. Perfect voters will be assumed to be positioned between all the cells in the network examples presented here. The effect of nonperfect voters can easily be included. However, it is more enlightening to assume perfect isolation between cells since our primary aim here is to compare the different cell models without getting into the question of effects due to voter reliability. The module dependent reliability model developed here which considers 0, 1, 2, and 3 module failures is also shown. Figure 5 shows the difference between the reliability model developed here and (2) and (3).

For convenience, the following conventions will be adopted for all the graphs now to be presented. In graphs displaying system reliability the fault equivalent model will be plotted as lines with a dash followed by a dot. The modified serial cell model (3) will be a solid line while the serial cell (2) is represented by a dashed line. For graphs depicting the difference in system reliability for the various models,, the difference between the fault equivalent model and the modified serial cell will be plotted as a solid line while the difference between the fault equivalent model and the serial cell model will appear as a dotted line.

For this case (3) is a fairly good approximation, although a bit pessimistic. Figure 6 illustrates the mission time improvement for the fault equivalent model over the serial cell model for the 15 NAND gate tree.

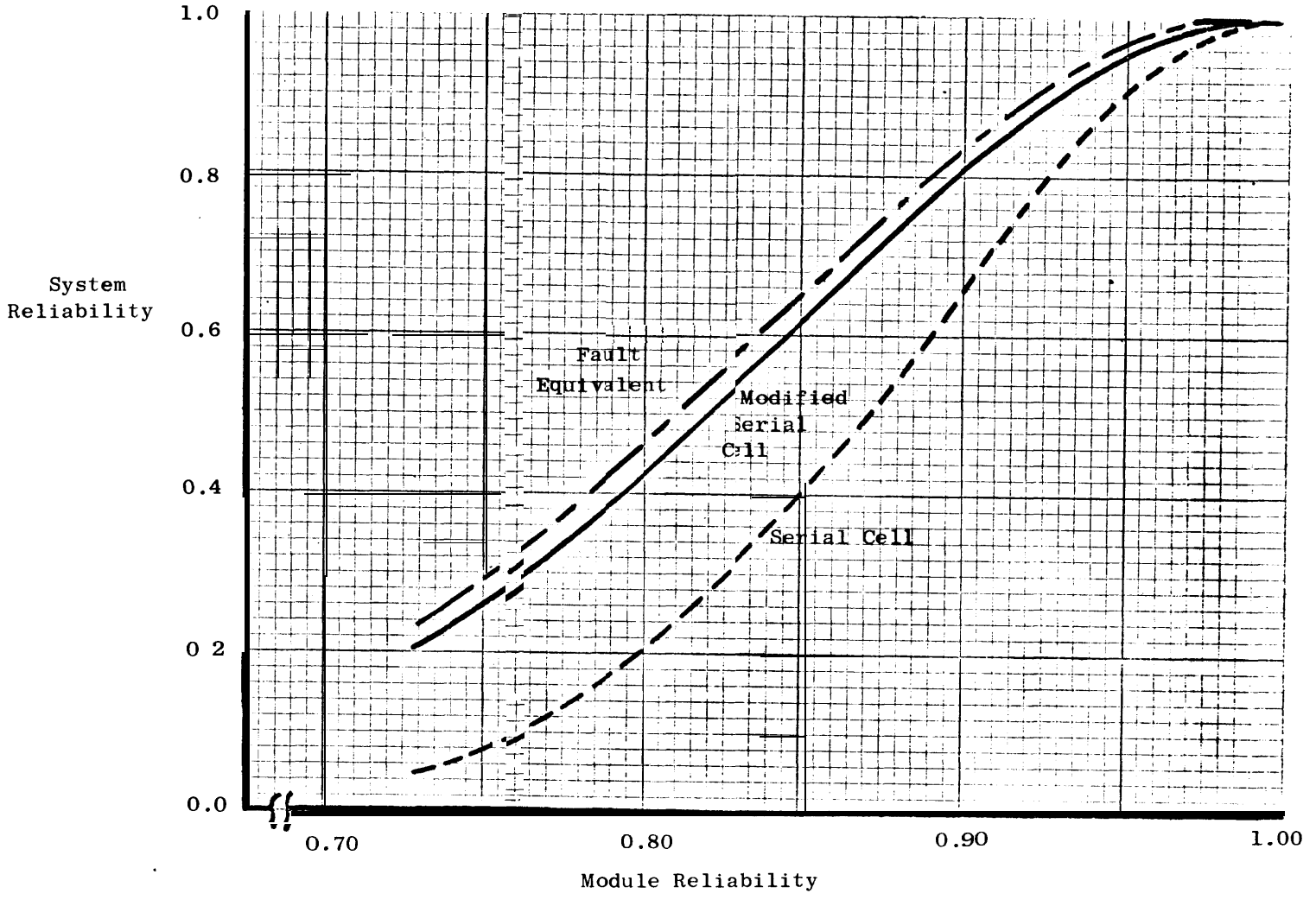


Fig. 4. The fault equivalent model, the modified serial cell (3), and the serial cell (2) reliabilities for the NAND cell of Fig. 3 in a TMR network of 15 cells.

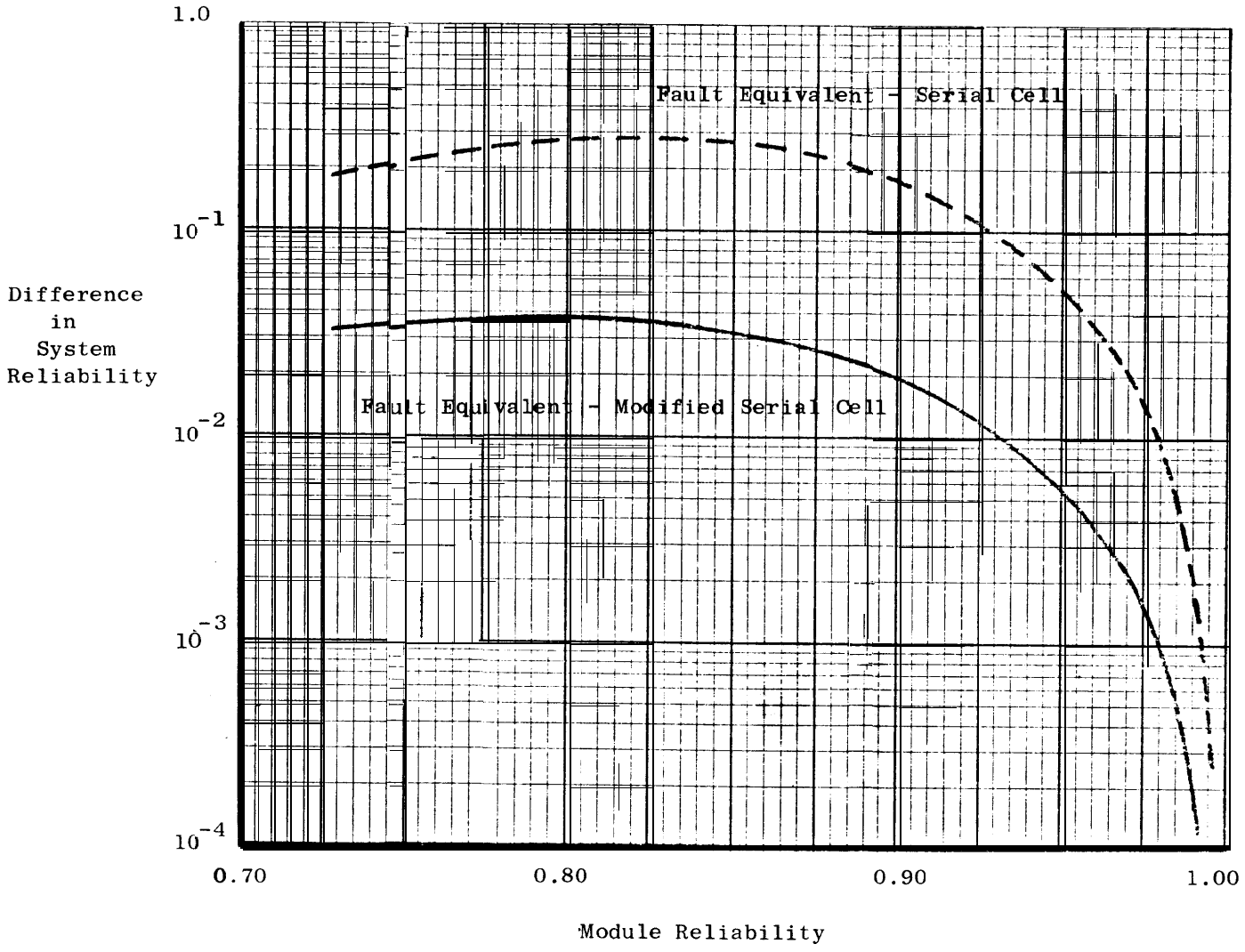


Fig. 5. The difference in system reliability between the fault equivalent model and the serial cell and the modified serial cell models for the NAND cell of Fig. 3 in a TMR network of 15 cells.

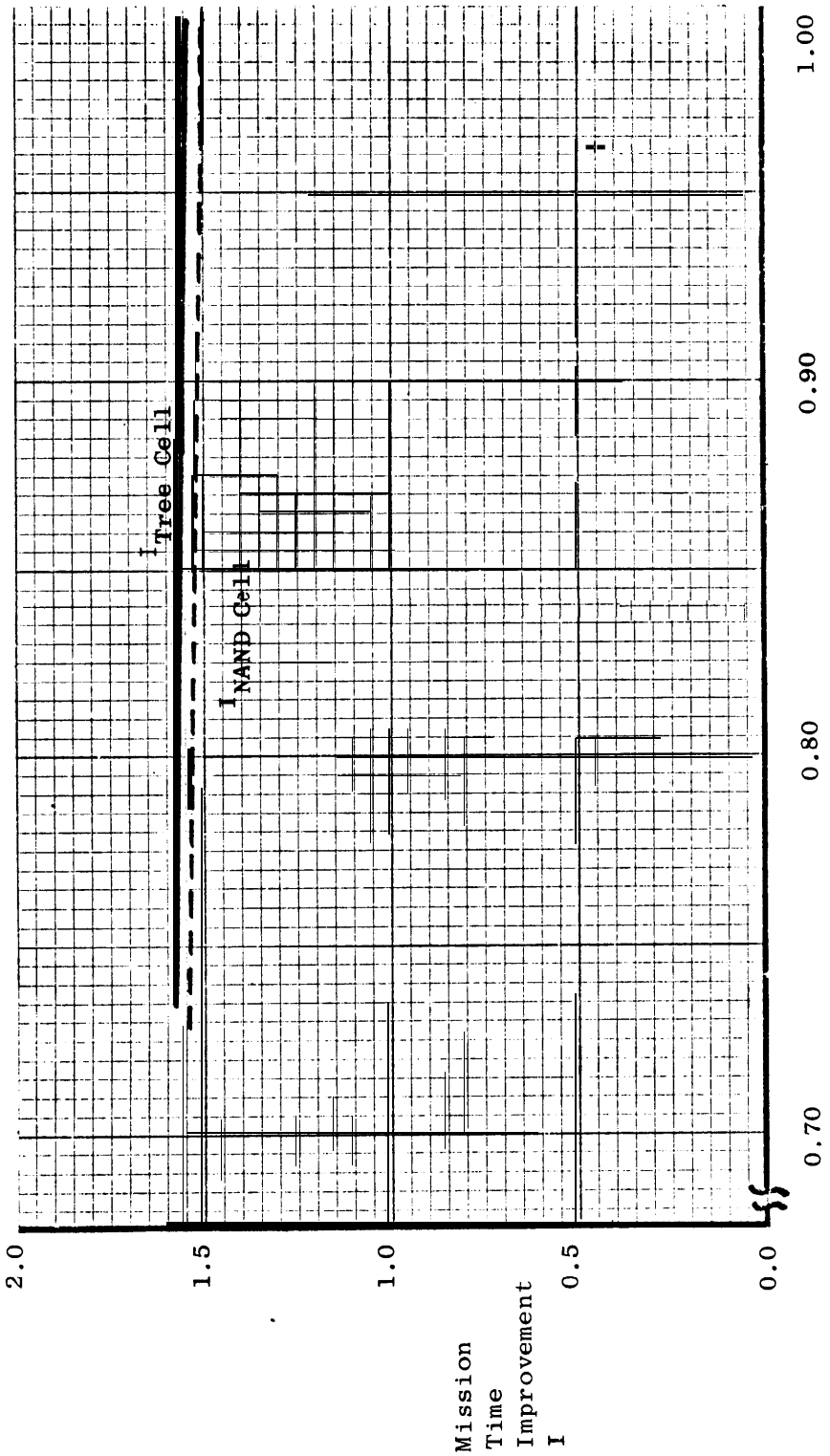


Fig 6 Mission time improvement for the fault equivalent model over the serial cell model. The networks are TMR with 15 NAND gate cells like Fig. 3 and 13 tree structure cells like Fig. 9.

The modified serial cell model with $K = 1/2$ will be demonstrated to be pessimistic for some networks and optimistic for other networks whose gates realize more complex functions than the elementary AND, OR, INVERT functions. Since a reliability model which is known to be a lower bound is more preferable than one whose behavior is unknown, the serial cell model was used for Figure 6. A 50% increase in mission time is obtainable by using the fault equivalent model.

The reliability models for the same network realized in five modular redundancy are shown in Figure 7 and their difference in Figure 8. For this case the factor K modifying the three module failure case is $6/8$ which was arrived at by assuming the only way for the network to fail was if all three failed modules agreed. If all trios of outputs from the three failed modules are equally likely then only 6 out of 8 do not lead to network failure. From Figure 7 we see that the modified serial cell model is not quite so good as before for this extremely simple example.

Figure 9(a) shows the logic diagram for a simple tree structure network and Figure 9(b) shows its logical model. The reliability models are compared in Figure 10 and 11 for a TMR network consisting of 13 of these cells arranged in three levels. K was selected as $1/2$ in the modified serial cell model. At $R_m = 0.90$ the reliability difference is 2.5% for the modified serial cell model (3) and 21% for the serial cell model (2). Figure 9 illustrates an I of about 1.5 for this network.

Finally, Figure 12(a) depicts a four input exclusive OR and Figure 12(b) displays its logical model. Figure 13 and 14 plot the reliability curves for a 64 bit parity tree utilizing the basic

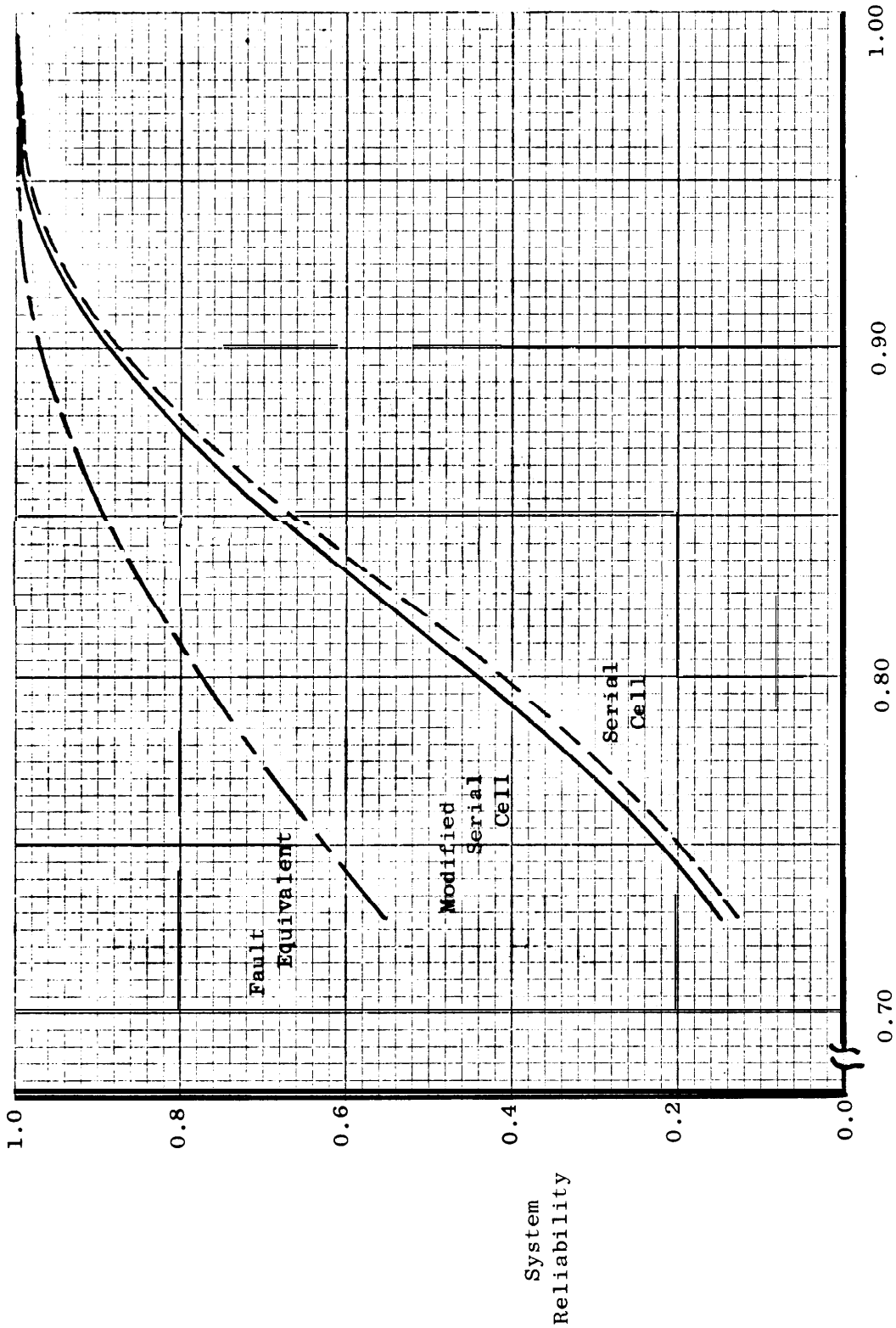


Fig. 7. The fault equivalent model, the modified serial cell (3), and the serial cell (2) reliabilities for the NAND cell of Fig. 3 in a five modular redundancy network of 15 cells.

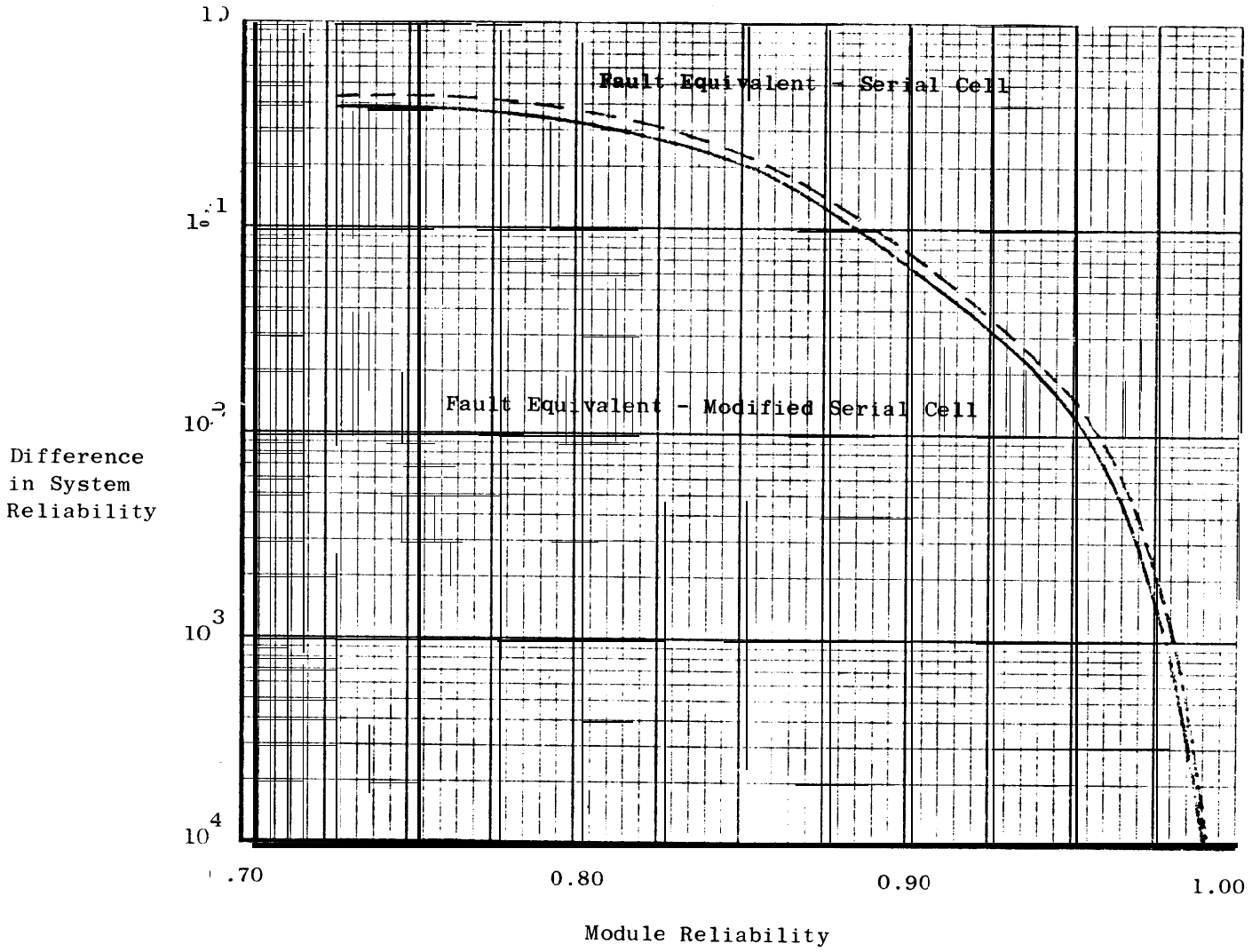
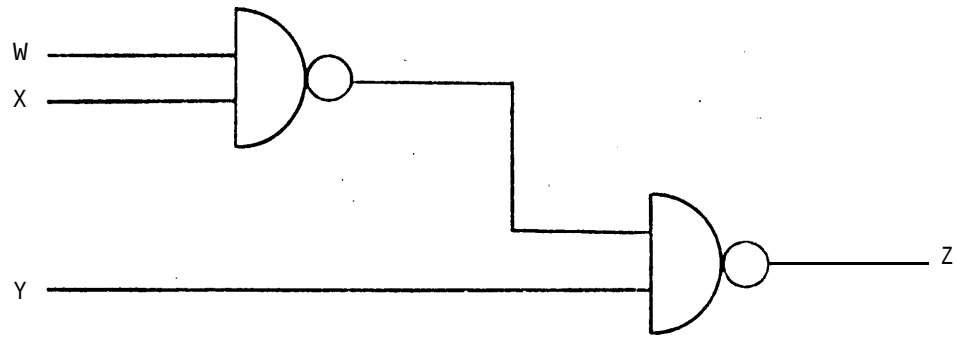
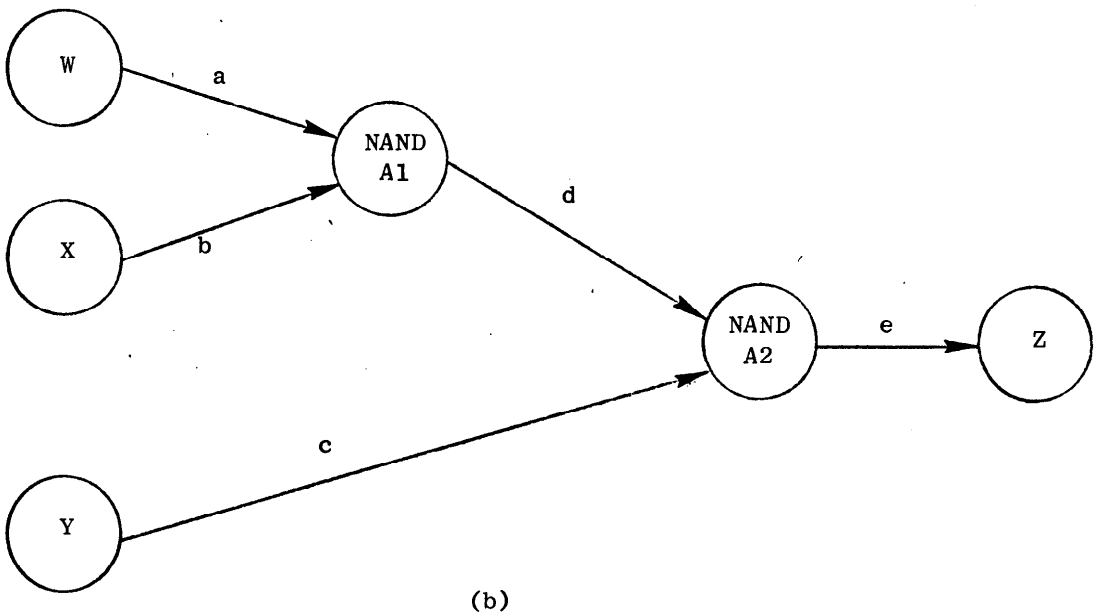


Fig. 8. The difference in system reliability between the fault equivalent model and the serial cell and the modified serial cell models for the NAND cell of Fig. 3 in a five modular redundancy network of 15 cells.



(a)



(b)

Fig. 9. The (a) gate realization and (b) the logical model for a tree structure cell.

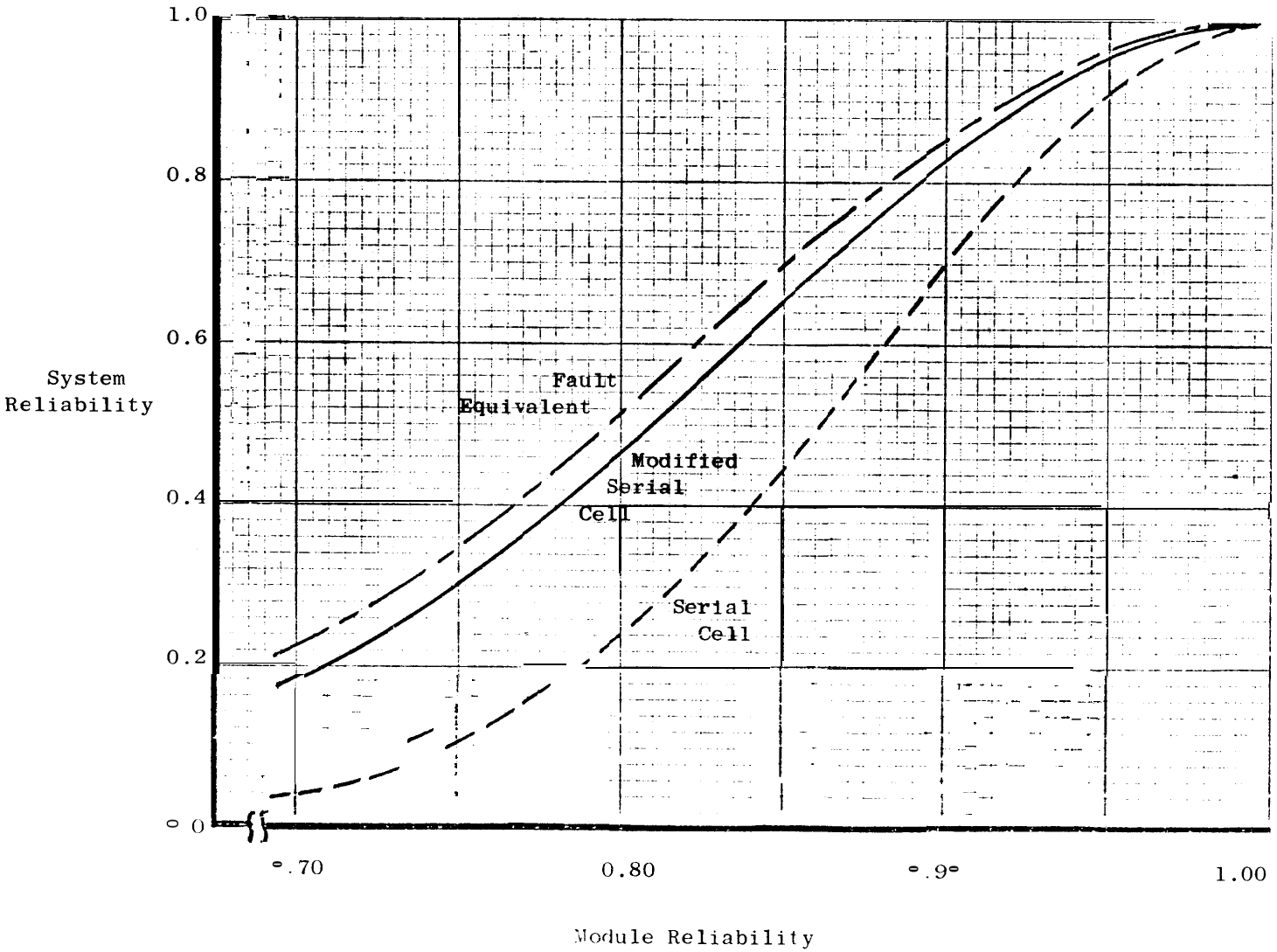


Fig. 10. The fault equivalent model, the modified serial cell (3), and the serial cell (2) reliabilities for the tree structure cell of Fig. 9 in a TMR network of 13 cells.

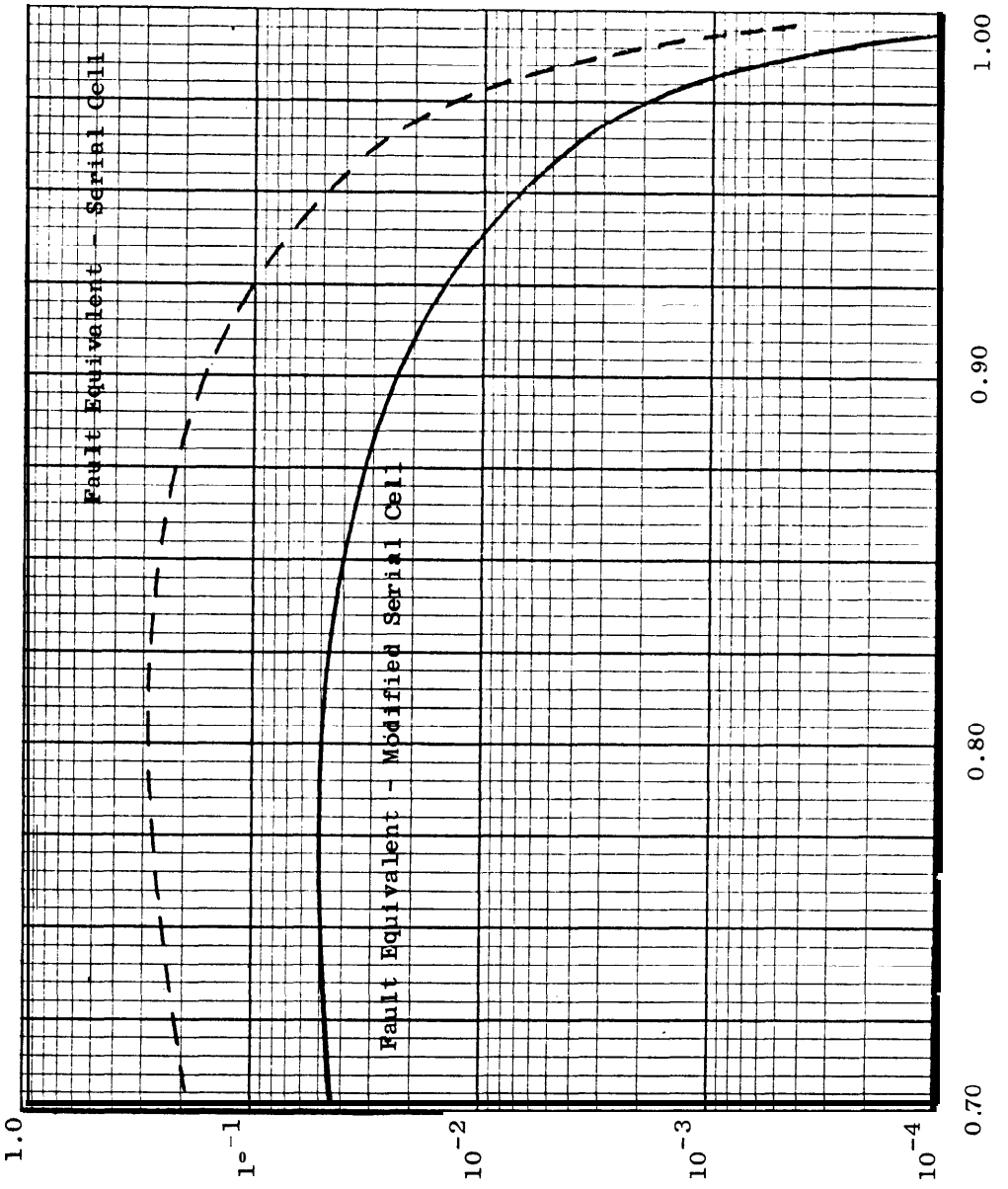
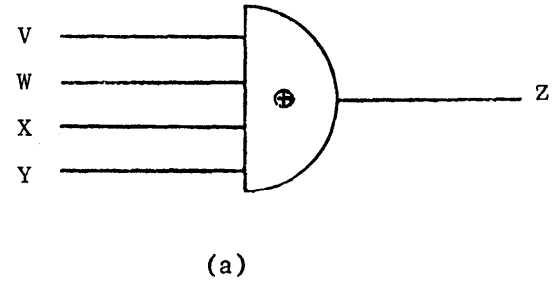
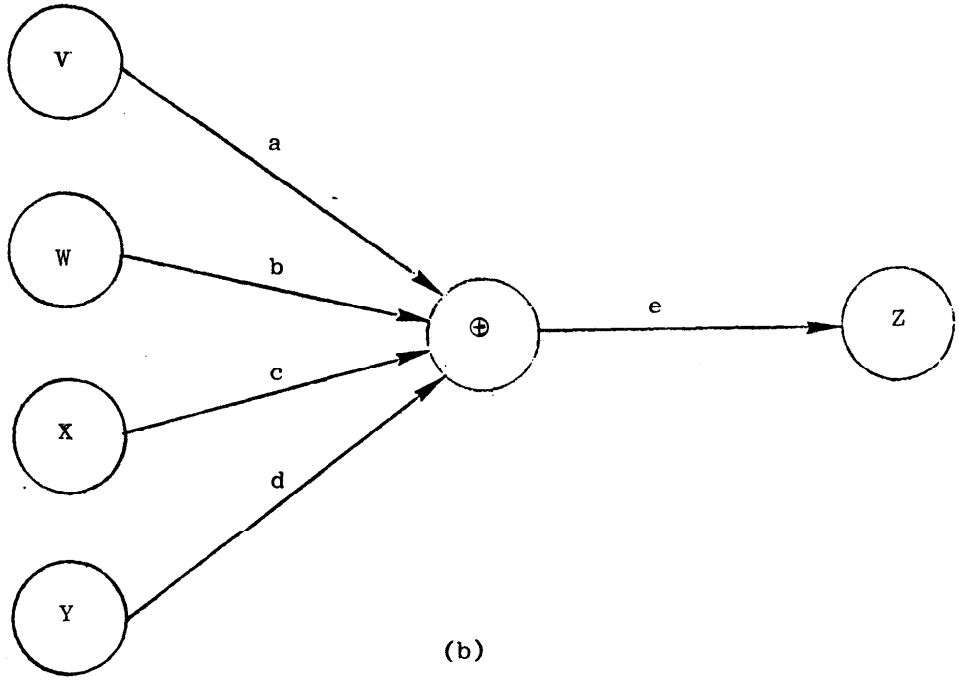


Fig. 11. The difference in system reliability between the fault equivalent model and the serial cell and the modified serial cell models for the tree structure cell of Fig. 9 in a TMR network of 13 cells.



(a)



(b)

Fig. 12. The (a) gate realization and (b) the logical model for a four input exclusive OR.

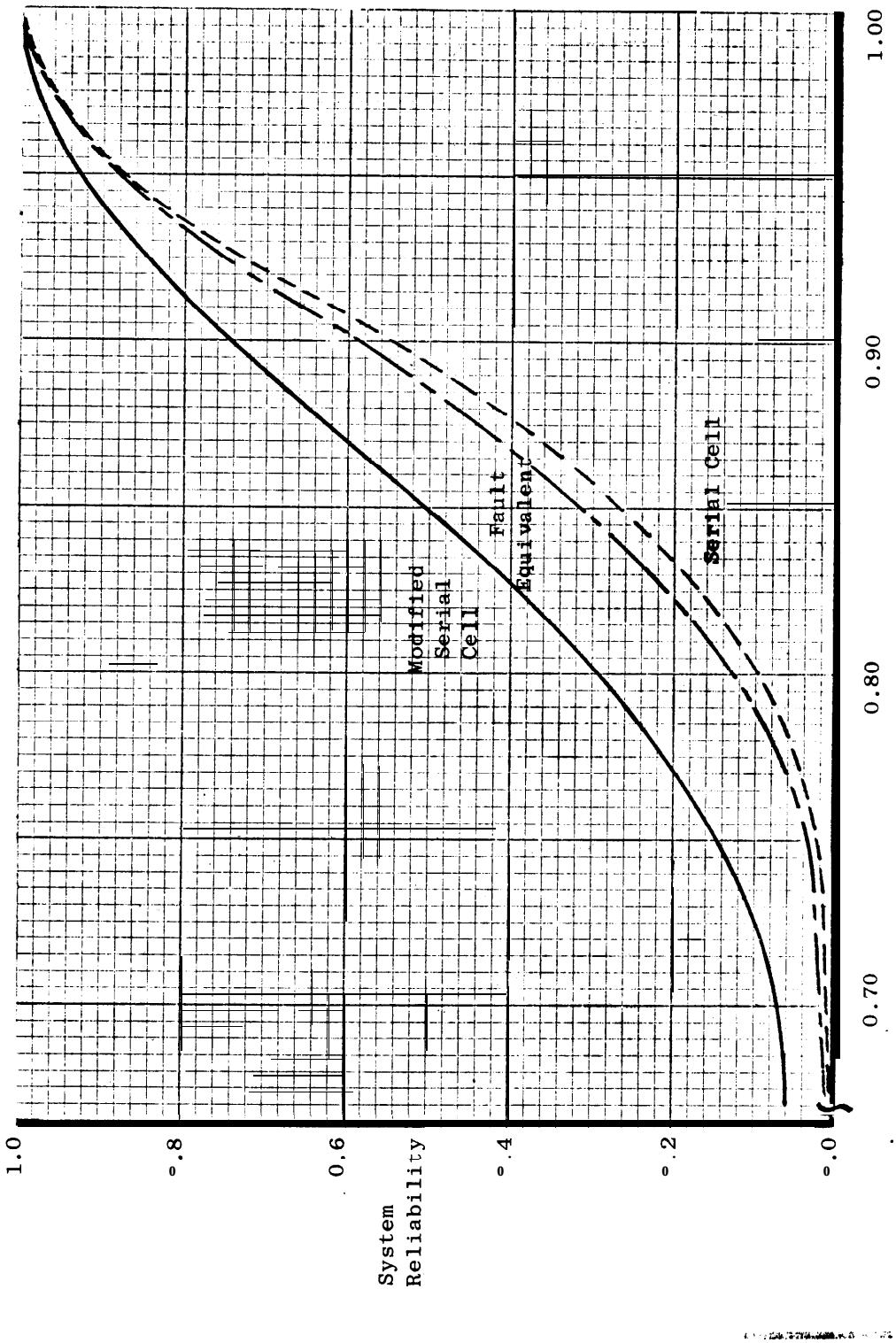


Fig. 13. The fault equivalent model, the modified serial cell (3), and the serial cell (2) reliabilities for the exclusive OR cell of Fig. 12 in a TMR network of 21 cells.

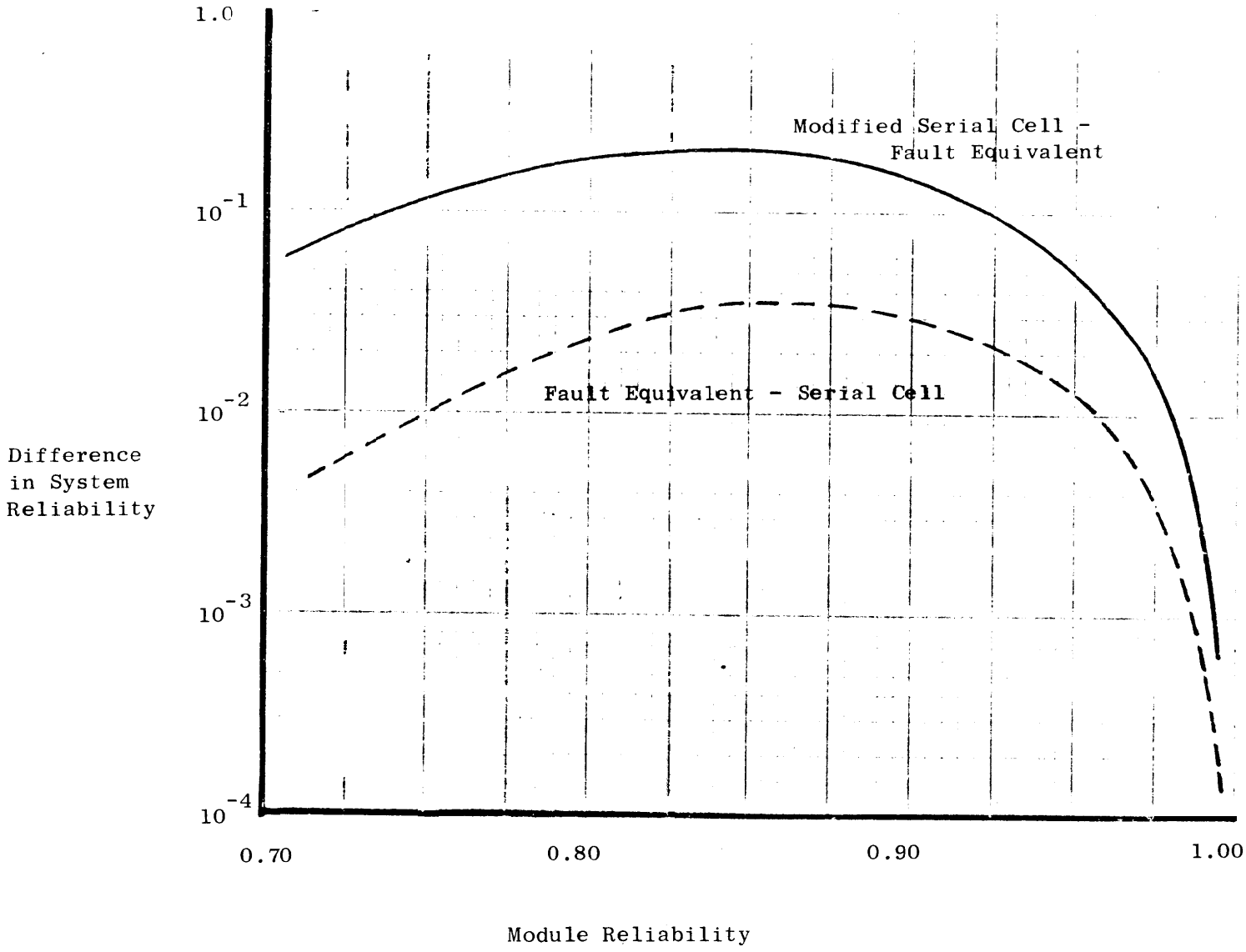


Fig. 14. The difference in system reliability between the fault equivalent model and the serial cell and the modified serial cell models for the exclusive OR cell of Fig. 12 in a TMR network of 21 cells.

cell of Figure 12. While the modified serial cell model was pessimistic in the networks previously presented, it is very optimistic for the parity tree and K = 1/2 can no longer be assumed to yield a lower bound as is done in the literature. For $R_m = 0.90$ the difference is almost 20%. This points out the serious error the modified serial cell model could introduce if modeling IC networks whose basic cell is a complex function and whose major source of failure is the input leads.

The fault equivalence matrix is the computational bottleneck for the fault equivalent (module dependent) approach. The calculational complexity, once the fault equivalence matrix is developed, is bounded by $(p \cdot n_F)^i$ where p is the number of leads in the module, n_F is the number of fault equivalence classes, and i is the number of failed modules under consideration. This is an upper bound since $p \cdot n_F$ is the number of elements in the E matrix and in the worst case every element in each E matrix representing a faulty module will have to be multiplied by every other element in every other failed module E matrix. A formula for n_F is given in [11]. This upper bound will normally be very pessimistic, For example, if two modules consisting of the two input NAND gate of Figure 3 were to fail, the upper bound predicts $(2 \cdot 5)^2 = 100$ multiplications when only 36 actual multiplications are needed.

In the module independent approaches, a reliability function, R_m, for the module was assumed. R_m must in turn be calculated. The fault equivalent model combines the computation of R_m with the computation of the system reliability. In fact, the same lead failure model might be used in developing R_m in the module independent approach.

Currently, research is underway to calculate the number of equivalence classes for an arbitrary network [11]. The task of developing the E matrix could also be aided by research into the size of equivalence classes. Also note that not all faults need be explicitly listed since some faults dominate other faults [12]. Consider faults with c/0 as a component (such as a/1, b/0, c/0) that will realize the same fault function as c/0. The number of triple faults realizing the constant 0 output function is rapidly calculated as $2.2 = 4$ since line a can be stuck at either 0 or 1 without affecting the output function and likewise for line b. Another way to cut down the computation is to consider only single line faults. This yields a slightly pessimistic reliability prediction since it assumes the only way a module can fail is via a single line stuck-at fault. Yet it may be entirely adequate for the desired application, especially if the line reliability is very high. This latter condition should hold for most cases.

CONCLUSIONS

We have seen that the classical model for modeling the reliability of multiple line redundancy techniques may be inadequate. The use of the fault equivalent model could produce a more accurate prediction of system reliability over wide ranges of module reliability for complex networks. The new module dependent reliability model could be of increased importance to the network designer if the majority of IC failure mechanisms become representable as line failures.

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