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MATHEMATICAL MODELS FOR THE CIRCUIT LAYOUT PROBLEM

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W. M. vanCleemput

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Stanford Electronics Laboratories

Stanford University
Stanford, California

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ABSTRACT

In the first part of this paper the basic differences between the classical (placement, routing) and the topological approach to solving the circuit layout problem are outlined.

After a brief survey of some existing mathematical models for the problem, an improved model is suggested. This model is based on the concept of partially oriented graph and contains more topological information than earlier models.

This reduces the need for special constraints on the graph embedding algorithm. The models also allow pin and gate assignment in function of the layout, under certain conditions.

MATHEMATICAL MODELS FOT THE CIRCUIT LAYOUT PROBLEM

1. Introduction

The circuit layout problem is an important facet of design automation of digital systems.[3] This problem is encountered in laying out printed circuit boards, integrated circuit masks, logic diagrams, flowcharts, electronic circuit diagrams, etc. This discussion will be limited to printed circuit board and integrated circuit layout.

The basic problem of laying out a circuit can be formulated as follows. Let $\mathcal{C}$ be a set of components C(i). Every component C(i) is itself a set of terminals i.e., $C(i) = \{t(i,j) , j = 1\ m(i)\}$, where m(i) is the number of terminals of component C(i) .

A net is a collection of terminals (of the same component or of different components) that have to be equipotential at all times. This is accomplished by connecting all the terminals of a net by a continuous strip of conducting material. The order in which the terminals of a net are to be connected is not specified in advance and can be chosen in function of an optimal layout, provided that certain physical constraints can be met (e.g. time-delay and cross-talk limitations).

Let N be the set of all nets N(j) . Each net N(j) is itself a set of terminals. The number of terminals of a net N(j) (or the cardinality of the set N(j)) will be denoted by p(j).

The circuit layout problem is then to position the components C(i) on a plane and to realize each of the nets N(j) on one or more planes, such that an objective function is minimized, thereby taking into account a number of constraints, Both the objective function and the constraints depend on the specific circuit layout problem being considered.

Geometrical versus Topological Information.

The topological aspects of the circuit layout problem relate primarily to the relative positions of components and interconnections. Other topological information includes the order in which the terminals of a component appear on its physical boundary as well as the possibility of routing connections under or over the area used by the component. The requirement that the external connections have to appear on the outside boundary of the circuit in a prespecified order is also a topological characteristic of the circuit layout problem. Sometimes, the order of terminals is not completely imposed upon the designer: e.g., the inputs of a three-input AND gate are interchangeable and a good layout procedure should take this into account.

The geometrical aspects of the circuit layout problem are related to parameters that can be measured. For layout problems one usually does not use the ordinary Euclidian metric, but rather the so-called Manhattan geometry, in which only vertical and horizontal line segments are allowed. The size of individual

components, the thickness of conductor lines and the size of a printed circuit board or an integrated circuit chip are examples of geometrical parameters.

An important geometrical characteristic is the concept of finte wiring capacities. These occur when the number of connectors in a given area is limited by geometrical considerations. Such is e.g., the case for the number of wires one can route between two adjacent terminals of a component.

The Classical Approach

Most procedures for solving the circuit layout problem first position the components thereby minimizing an objective function. This function should be a measure of the quality of the final layout. Usually the total wirelength is the parameter one tries to minimize. This tends to cluster together heavily connected components and to shorten the longest wires, which are desirable side-effects. Once the placement is obtained, it is frozen and the routing of connections has to be performed within this fixed-component topology.

Gate assignment is usually done before the placement phase while pin assignment is often deferred until the interconnection routing phase.

An excellent survey of component placement techniques is contained in [18].

The routing of interconnections is frequently done sequen-

tially using algorithms such as Lee's [25] or Hightower's [21]. Sequential routing inherently raises the question of selecting the order in which interconnections should be routed, This problem was studied in [1].

Algorithms that allow some degree of parallellism in the routing phase were proposed in [20] and [26], although these algorithms are applicable only to a restricted class of problems.

The interconnection routing problem is surveyed in [1] and [27].

The reason why the circuit layout problem is partitioned into independent subproblems such as placement, assignment and routing is primarily because of the computational complexity of the global problem.

In the classical approach, both the topological and the geometrical aspects of the circuit layout problem are not fully taken into account. In the routing phase it may be impossible to route a connection in a given routing plane. This failure may be caused by one of the following:

1) Congestion: An interconnection cannot be routed because of limited wiring capacities (geometrical constraint).
2) Topological obstruction: Some connections may be routed in topologically different ways. However, choosing a particular topological embedding may reduce the ability to route other connections. This problem is illustrated in Fig. 1, where four components, labeled A, B, C and D are connected by two nets $\{2,7\}$ and $\{1,3,4,5,6,8\}$.

The layout shown in Fig. l(a) shows the possibility of embedding both nets in the same plane. In Fig. l(b) the net $\{1,3,4,5,6,8\}$ has been embedded differently, thereby making it impossible to embed $\{2,7\}$ in the same plane.

3) Inherent non-planarity: No embedding in the plane exists.

This classical approach has proven successful in the layout of multilayer printed circuit boards with a regular structure. When multiple interconnection layers are available and when a given interconnection can be realized in more than one layer (through the use of vias), then the occurrence of topological obstructions is not of a critical nature. Furthermore total completion of all interconnections, although desirable, is not essential for printed circuit boards.

The Topological Approach

The main concern in solving the circuit layout problem is to embed the connections in one or more planes, such that no two connections intersect. This criterion shows a striking similarity with the planarity concept in graph theory*: a graph is planar if it can be embedded in the plane such that no two edges intersect.

The topological approach is based on graph-theoretical concepts and first constructs a graph model for the circuit. This graph represents the topological aspects of the circuit as

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* Unless otherwise defined, all graph-theoretical terms follow Harary [19].

faithfully as possible, while neglecting all geometrical information. This graph then is embedded in one or more planes. If some of the connections remain unembedded, one attempts to route them by making use of technological properties. The final step consists of transforming the topological layout into a physical layout, that takes into account the geometrical properties.

In this approach, the topological parameters are considered at all stages, while the geometrical information is used only in the last phase of the layout.

Although several attempts were made to solve the circuit layout problem using graph-theoretical methods, working systems have appeared only recently.

Topological methods for laying out one-sided printed circuits were proposed by Kodres [23] and Weissman [39]. Methods for the layout of thin film RC circuits were mentioned by Sinden [29,30] and Bedrosian [6]. Weinberg [38] discusses graph-theoretical concepts such as planarity and isomorphism, that are useful for solving circuit layout problems. Akers and Hadlock [4] describe a layout method for IC's based on a graph-theoretical method. Akers, Geyer and Roberts [3] continue this approach and also describe a method to transform the topological embedding into a physical layout, which takes into account the actual dimensions of the components, A good survey of the topological approach to the circuit layout problem is given by Kodres [24].

Working systems for the layout of integrated circuits, based on a graph-theoretical approach are described by Yoshida and Nakagawa [40], Engl and Mlynski [7,8,14], Fletcher [16], Klamet [22] and Sugiyama [31]. An effort to justify theoretically the models used is given by Engl and Mlynski [10,11,12,15] and by Vanlier and Otten [37].

One serious objection to topological layout methods is that they usually do not take into account any physical parmeters, such as the number of wires one can route between two adjacent pins of a component or the capacity of a routing channel. As was indicated in [36], it is possible to take some finite capacities into account in a graph-theoretical model.

Some interesting results on transforming a topological embedding into a physical layout were reported by Zibert and Saal [41], [42].

Many existing systems for topological IC layout are limited to small-scale circuits. Because of the inadequacy of the models and algorithms employed, they often rely heavily on interaction for obtaining a final layout.

In the next section some of the existing models will be critically discussed while in section 3 the properties of physical circuits will be studied, emphasizing those properties that are relevant to solving the circuit layout problem.

2. Some Existing Mathematical Models.

In the previous section it was pointed out that the first step in a topological layout procedure consists of constructing a graph model for the circuit. This model should reflect the topological properties of the circuit such that in the subsequent steps an optimal layout may be obtained.

An abstract model was proposed recently by Engl and Mlynski [15]. From this model a graph can be derived for the embedding step.

This abstract model is based on the following concept: A multiplace graph is a pair G(A,R), where A is a finite set of vertices and R is a family of multisets* defined on A. Each element of R is an edge of the multiplace graph.

Engl and Mlynski proposed the following model for the circuit layout problem:

- Nets are represented by vertices of the multiplace graph.
- A n-terminal component is modelled by an edge of the multiplace graph i.e. a multiset of cardinality n.

This multiplace graph is called the potential graph of the circuit.

The transpose of a multiplace graph G(A,R) is another multiplace graph G'(A',R') which has as its incidence matrix the transpose of the incidence matrix of G. The transpose of the potential graph is called the component graph. Here the components are represented by vertices and the nets by multisets.

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* A multiset is also known as a weighted set.

In the potential graph, a component with n pins is modelled by a multiset of cardinality n. The reason why multisets are needed to model a component is that more than one terminal of a component can be connected to the same net, For the same reason multisets are needed to model nets in the component graph. It is not possible to represent the relationships that exist between the pins of a component with this model.

The concept of planarity of a multiplace graph is related to the mapping of a multiplace graph M(A,R) into a simple graph G(V,E): every element of the set A is mapped into a distinct vertex of the graph G. Every element x of R is mapped into a K(1,n) (i.e. star-) subgraph, with the center vertex representing the element and the edges representing the fact that some vertices of A belong to x.

This mapping can result in a graph with multiple edges. A multiplace graph is planar if the corresponding simple graph is planar. Since multiple edges do not influence planarity, they can be replaced by a single edge.

Mapping the potential graph into a simple graph results in modelling a net by a vertex and a component by a star, which is homeomorphic to the model proposed in [4a]. Mapping the component graph results in modelling a net by a star and a component by a vertex, which is the model of [17]. It should be noted that both the potential graph and the component graph map into the same bipartite graph.

This model may be planar when the actual circuit is not and vice versa, as shown in Fig. 2.

Several other graph models were proposed. In [40] components are modelled by vertices and nets by edges. This requires a prior decomposition of every net into simple interconnections and does not allow this to be done in function of an optimal layout.

Several authors [37, 5, 28] propose the representation of a component by a cycle. This may lead to an embedding in which a part of the graph is embedded inside a cycle representing a component. This can be prevented by placing a star inside the component [37], thereby forcing the cycle to be a face when the star is removed from the embedding.

Another problem that may occur is that the embedding results in a plane graph in which the mirror image of the cycle occurs. In printed circuit technology this means that the component should be placed on the other side of the board, which is clearly inacceptable. In [37] it is proposed that the embedding algorithm take care of this constraint.

None of the existing models take into account all the properties of physical circuits that will be discussed in section 3. Furthermore they require the embedding algorithm to be aware of a number of constraints that essentially are of a topological nature. E.g. that the external connections have to be placed on the periphery of the circuit; that the cycles representing components be embedded with a certain orientation; that the external

connections have to appear in a certain order on the periphery.

The rest of this paper will be devoted to developing a model that 1. includes those topological constraints.

2. takes into account certain properties of physical circuits.

3. Properties of Physical Circuits.

In this section a number of properties of physical circuits useful in solving the circuit layout problem optimally will be discussed.

Let $\mathcal{C} = \{C(i)\}$ be the set of components.

For solving the circuit layout problem it is desirable to distinguish between the different terminals of a component since this leads to a better layout.

A component C(i) can be considered a set of terminals t(i,j). Let $\mathcal{T}$ be the set of all terminals. Note that $C(i) \cap C(j) = \emptyset$ for $i \neq j$ and

$$\bigcup_{i=1,|\mathcal{C}|} C(i) = \mathcal{T}$$

The set of components $\mathcal{C}$ is a family of subsets of $\mathcal{T}$.
Consider the set of all terminals: between two terminals that belong to the same net, there exists a relation "are interconnected". This relation is reflexive, symmetric and transitive and therefore is an equivalence relation. This equivalence relation partitions

the set $\mathcal{T}$ into a number of disjoint subsets (equivalence classes) called nets, A net N(k) is a subset of $\mathcal{T}$. Again $N(i) \cap N(j) = \emptyset$ for $i \neq j$.

When a terminal T(i,j) is not connected to any other terminal, then it belongs to a net N(i) of cardinality 1. Such nets are degenerate. Proper nets are of cardinality 2 or greater. The total wiring&et of all nets) is again a family of subsets of $\mathcal{T}$.

Relations between the Terminals of a Component: Cyclical Ordering.

In many cases, the order in which the terminals of a component appear on the periphery of this component is predefined. This can be represented by defining a function S(i), called the successor function for a component i. This function S(i) maps a terminal t(i,j) of C(i) into another terminal t(i,k) of C(i). This mapping is one-to-one. The inverse function R(i), called the predecessor function, also maps every terminal of C(i) into another terminal of C(i).

Relations between the Terminals of a Component: Physical Equivalence of Terminals.

By the physical equivalence of a set of terminals of a component is meant that all terminals in this set are equipotential. This means that a net can be connected to any one of these terminals.

As an example of this, consider an IC transistor: topologi-

cally, one should consider this as a 6-terminal component, with opposite terminals being physically equivalent, as shown in Fig. 3.

Let F be a subset of C(i), consisting of terminals that are physically equivalent, At least one of these terminals has to be connected to a net N(k). Each group of physically equivalent terminals of component i can be represented by a set F(i,j), with $|F(i,j)|$ at least equal to 1. Component i can be represented by the set C(i) = $\{F(i,j)\}$.

Relations between the Terminals of a Component: Logical Equivalence of Terminals.

It often occurs that a number of terminals of a component have identical logical functions; this allows terminals to be interchanged in order to obtain a better layout. An example of such a situation is an AND gate with 3 inputs: suppose that each of the terminals has to be connected to a net, one should not a priori assign a net to a physical terminal but rather do this in function of an optimal layout. This problem is often referred to as the pin assignment problem.

Let L be a subset of C(i), consisting of terminals having identical logical functions. Each of these terminals is incident with a net N(k). Since the terminals in the set L all perform identical logical functions, it is permissible to assign the nets N(k) to any permutation of the terminals t(i,j). The terminals in the set L are logically equivalent.

Each group of logically equivalent terminals of a component i can be represented by a set L(i,j) of terminals, The cardinality of each such set is at least 1. We can represent component i by a set $C(i) = \{L(i,j)\}$.

It is possible that within a component both physical and logical equivalence of terminals exists, In that case, the following property holds: if $t \in F(i,j)$ and $t \in L(i,k)$, then for all elements $t \in (F(i,j) : t \in L(i,k)$.

Relations between the Terminals of a Component: Subcomponent Equivalence.

In some cases, a component can be made up of a number of identical subcomponents, that are logically interchangeable. As an example of this is a quadruple 2-input NAND gate, which is a common IC module available commercially. Another example is a 3-3-3 AND-OR-INVERT gate (Fig. 4).
In such cases, one should not randomly assign a physical component to a particular group of nets to be connected to one such subcomponent, but rather do this in function of an optimal layout.

This can be modelled by representing component i by a collection of sets of equivalent subcomponents $C(i) = \{E(i,j)_4$,where $E(i,j) = \{L(i,j,k)_4$, i.e., each subcomponent consists of a set of logically equivalent terminal sets L(i,j,k); furthermore $L(i,j,k) = \{F(i,j,k,l)\}$ i.e., each set of logically equivalent

terminals consists of a set of physically equivalent terminal sets, and finally $F(i,j,k.l) = \{t(i,j,k,l,m)\}$ i.e., each set of physically equivalent terminals consists of one or more physical terminals.

4. Representing Nets

As was mentioned before, a net is a collection of terminals that have to be equipotential at all times, The order in which the terminals are connected is not a priori defined and may be chosen in functions of the layout.

Assuming that every terminal is represented by a distinct vertex, then any spanning tree on the n vertices of the n-terminal net would be a satisfactory solution. Unfortunately there are n^{n-2} possible spanning trees on n vertices. In order to find an optimal layout one would have to enumerate all possible combinations over all nets. This is clearly impractical.

On the other hand, an a priori arbitrary decomposition of the net into simple (two-point) interconnections- as proposed in [40] may lead to a far-from-optimal layout.

A compromise solution is to represent a net by a single vertex. Several authors (e.g. [14], [37]) propose a represen - tation that results in a single vertex, not only modelling the net but also all terminals belonging to that net. This can lead to difficulties in identifying individual terminals in the embedding step.

The most appropriate model is a star as proposed by Goldstein and Schweikert [17]. This will not always result in an optimal decomposition of the net, as illustrated in Fig. 2(c,d) where a planar circuit results in a nonplanar graph model. However, modelling a net by a star appears to be the only feasible solution not requiring the enumeration of all possible combinations of net decompositions, In the following sections it will therefore be assumed that nets are modelled by stars.

5. Graph Models for Components.

It will be assumed here that nets are modelled by stars (see section 4). Furthermore, it will be required that nets be embedded in the region exterior to a component's boundary and that no mirror-image equivalents of components are available.

We will introduce the following terminology here before examining graph models for components.

Let G(V,E) be a graph with a vertex set V and an edge set E. The neighborhood N(v) of a vertex v of G is the set of all vertices of G that are adjacent to v.

An orientation o(v) of a vertex v of G is a cyclic permutation of the elements of the neighborhood of v.

An orientation O(G) of a graph G is a mapping of the vertex set V into the set of orientations of all vertices of G.

The triple (V,E,O) is an oriented graph.*

A graph G(V.E.O) is partially oriented if the mapping of V into the set of orientations is partially defined (i.e. O(G) is defined for a proper subset of V only).

An oriented vertex is a vertex for which an orientation is defined.

A graph G with p vertices and q edges is planar (i.e. embeddable in a plane S) if it is possible to associate a collection of p distinct points of S (corresponding to the vertices of G) and a collection of q Jordan arcs (corresponding to the edges of G), such that if an arc "a" corresponds to an edge e=$\{u,v\}$,

* The concept of oriented graph was introduced by Ulrich [32]

then only the endpoints of "a" correspond to vertices of G (i.e. u and v).

A plane graph is a graph that is embedded in the plane.

A region or a face of a plane graph G is a maximal portion of the plane forwhich any two points may be joined by a Jordan arc "b", such that any point of "b" neither corresponds to a vertex of G nor lies on a Jordan arc corresponding to an edge of G.

The boundary of a region R of a plane graph consists of all the points x corresponding to vertices of G or lying on a Jordan arc corresponding to an edge of G such that x can be joined to a point of R by a Jordan arc all of whose points (except for x) belong to R.

A graph G is outerplanar if it can be embedded in the plane such that every vertex of G lies on the boundary of the same region (usually the exterior).

Let G(V,E) be a graph and let V_1 be a subset of V, then G is outerplanar with respect to V_1 if it can be embedded in the plane such that all vertices of V_1 lie on the boundary of the same region.

A partially oriented graph G is planar if it can be embedded in the plane such that for the arcs a(i) with a common endpoint P, that-correspond to the edges incident to a given vertex v, a clockwise sweep around P encounters these arcs a(i) in the order prescribed by the orientation.

It should be noted that with every plane graph, one can associate an oriented graph. However, not every oriented graph

has a corresponding plane graph (i.e. is planar).

Desirable Properties of an Adequate Component Model.

1) In order to avoid introducing non-planarities a graph model for a component should be outerplanar with respect to the vertices, that represent the component's terminals.

2) Every possible embedding of the component together with the nets connected to it should be compatible with the cyclical ordering of the terminals on the component% boundary. In other words, every possible embedding must have a physical meaning.

Cyclic Ordering of the Terminals.

In section 3 it was mentioned that the ordering of terminals along a component's boundary can be modelled by a successor function. This cyclic relationship can be represented by a cycle.
When we assume nets to be embedded in the region exterior to the component's boundary and if the nets are represented by stars then we can model a component and its incident net-edges by a partially oriented graph G, as shown in Fig. 5(a). The vertex set of G consists of oriented vertices, representing terminals and of non-oriented vertices, representing the nets. The edge set of G consists of a cycle, modelling the component's boundary and of edges, connecting the terminals to the net-vertices.

Physical Equivalence of Terminals.

Consider a component $C(i) = \{F(i,j)\}$ where $F(i,j)$ is a set of

physically equivalent erminals. Then $|F(i,j)| \geq 1$ and $F(i,j) \cap F(i,k) = \emptyset$ if $j \neq k$.

It will be assumed here that no two elements of F(i,j) are physically adjacent, If two or more terminals are physically adjacent, there is no problem of pin assignment between them and they can be represented by a single terminal.

Consider the partially oriented graph G', obtained from the original graph G by contracting the sets of physically equivalent terminals. The vertex set of G' consists of vertices, representing the sets of physically equivalent terminals and of vertices, representing the nets. The edge set of G' consists of the edges, connecting the terminals to the corresponding net-vertices and of edges representing a relation between physically equivalent sets. An example of this is given in Fig. 5(b), where the sets X and Y of physically equivalent terminals are contracted. A vertex corresponding to a set F(i,j) of cardinality greater than 1, must be non-oriented, on order to allow the incident net-edge to be embedded properly. The vertices, corresponding to sets F(i,j) of cardinality 1, remain oriented.

In order for the resulting model to be suitable, every possible embedding must have a physical meaning. From Fig. 5(b) it can be seen that the net connected to the set X can be embedded in two different ways, corresponding to assigning the physical net to either terminal 2 or to terminal 9. Fig. 6 shows an example where this pin assignment is critical for

the net connecting terminals lc, 2a and (3b or 3e). If the net had been a priori assigned to terminal 3e then no solution exists as shown in Fig. 6(a). By using a model as described above, the solution of Fig. 6(b) would be obtained.

[3]

Another condition to be met by the resulting model is that it has to be outerplanar with respect to the set of vertices that represent terminals. This condition can be verified as follows.

Consider the partially oriented graph G, with a cycle modelling the component's boundary and with oriented vertices representing the terminals and non-oriented vertices representing the nets as shown in Fig. 5(a). We can then construct a new graph G' as follows.

-For every set $F(i,j) = \{t(i,j,k)\}$ of cardinality greater than 1, we add a star subgraph to the model, with a new vertex $d(i,j)$ being the center, connected to the vertices $t(i,j,k)$ such that $d(i,j)$ lies between $c(i,j,k)$ and $a(i,j,k)$, where $t(i,j,k) = S(a(i,j,k))$ and $c(i,j,k) = S(t(i,j,k))$. If the oriented graph so obtained is outerplanar, then the graph derived by contracting all the $K(1,n)$ subgraphs is also outerplanar. Fig. 5(c) shows the graph G' corresponding to the graph G of Fig. 5(a).

Logical Equivalence of Terminals.

Let $C(i) = \{ L(i,j)\}$, where $L(i,j)$ is a set of logically equivalent terminals. Then $|L(i,j)| \geq 1$ and $L(i,j) \cap L(i,k) = \emptyset$ if $j \neq k$.

Consider a set $L(i,j) = \{t(i,j,k)\}$ of terminals with identical logical functions, Each of the terminals $t(i,j,k)$ is incident with a net N(1). The component model should be outerplanar and for every permutation of the terminals, the cyclic ordering should be respected.

Let G be the partially oriented graph, representing the component boundary and its incident net-edges, We can then consider the partially oriented graph G', obtained by contracting the sets $L(i,j)$. The vertices of G', corresponding to sets $L(i,j)$ of cardinality 1 remain oriented. An example is shown in Fig. 7.

In order to perform pin assignment in function of the layout the orientation of the nets around a vertex corresponding to a set $L(i,j)$ of cardinality greater than 1 should not be specified. This can be accomplished by inserting an edge for every set $L(i,j)$ of cardinality greater than 1, as shown in Fig, 7(c). Let $G[L(i,j)]$ be the subgraphs of the cycle, generated by the subsets $L(i,j)$. Then there exist two possibilities:

1) All of the subgraphs $G[L(i,j)]$ are connected. This implies that the vertices of $L(i,j)$ are physically adjacent. Then the new graph G' remains 2-connected, A vertex in G', corresponding to a set $L(i,j)$ of cardinality n, will then be connected to n nets. Assuming that the total circuit layout graph is planar, then every possible embedding will satisfy the requirements.

2) At least one of the subgraphs $G[L(i,j)]$ is disconnected. This implies that the vertices of L(i,j) are not all adjacent. As a result the graph G' is l-connected and if the set L(i,j) has cardinality n, then the corresponding vertex will be connected to n nets. Not every possible embedding however satisfies the requirements.

Therefore , this model is appropriate for logical equivalence, if all logically equivalent terminals are physically adjacent. Fig. 8 shows an example where the modelling of logical equivalence may result in a better layout. Assume that the terminals a,b and c of component 1 are logically equivalent. Fig. 8(a) shows a non-planar layout resulting from assigning nets arbitrarily to the terminals of component 1. Fig. 8(b) shows a planar layout that may be obtained by using an appropriate graph model.

It should be pointed out here that it may be possible to model logical equivalence even if the terminals are not physically adjacent.

Unspecified Order of Terminals.

In some cases, the components can be (re-) designed if this Would result in a better layout. From the point of view of circuit layout, this property is similar to logical equivalence of terminals.

In case the order of all terminals is unspecified, the

component can be represented by a single undirected vertex (or by a star subgraph if one desires a distinct vertex to represent each terminal). This results in a model, similar to the one proposed by Engl and Mlynski [14]

Logical Equivalence of Subcomponents.

Let C(i) be a component, consisting of n sets E(i,j) of logically equivalent subcomponents.

In the following discussion, we will impose the following restrictions:

1) a subcomponent is a collection of physically adjacent terminals, performing a specified logical function.
2) In order for 2 subcomponents to belong to the same set E(i,j), they have to perform identical logical functions, have the same number of terminals and the order in which the terminals appear on the component's boundary must be the same.

Consider the partially oriented graph model G for the order of the terminals on the component's boundary, as illustrated in Fig. 9 (a) and 10(a). Let G[S(i)] denote the subgraph G, generated by a subcomponent S(i). Since we require the terminals of a subcomponent to be physically adjacent, all G[S(i)] are connected paths. Let x(i) and y(i) be the vertices of valency 1 of G[S(i)], such that y(i) = S+(x(i)). * Let $x_1(i)$ be the vertex preceding x(i)

* By a=S+(b) we will denote that a was obtained from b by multiple application of the successor function S.

i.e. $x(i) = S(x_1(i))$ and let $y_1(i)$ be the vertex following $y(i)$ on the original cycle i.e. $y,(i) = S(y(i))$. We now derive a new graph model G' for the component as follows.

$$V(G') = V(G) \cup \{a(i)\}$$

$$E(G') = E(G) - \{(x_1(i),x(i)),(y(i),y_1(i))\}$$
$$\cup \{(x_1(i),a(i)),(a(i),y_1(i)),(a(i),x(i)),(a(i),y(i))\}$$

where a(i) is a new vertex, associated with subcomponent S(i).

By repeating this for every subcomponent S(i) with more than 1 terminal, we obatin a new oriented graph model G". For the purpose of embedding, G" is iquivalent to the original model G. Examples are given in Fig. 9 (b) and 10 (b).

"'As a result of this transformation, the graph model now consists of a cycle for the component itself and of cycles for each of the subcomponents, The cycle modelling the component itself, contains vertices that represent terminals as well as vertices a(i) for each subcomponent.

Let $E(i) = \{S(i,j)\}$ be a set of subcomponents with identical logical functions. Let every subcomponent S(i,j) be connected to a collection N(i,j) of nets. The component model to be derived should be outerplanar and every permutation of the logically equivalent subcomponents, allowed by the graph model should have a physical meaning i.e. be compatible with the cyclical ordering of the terminals.

We can now consider the oriented graph, obtained by contrac-

ting the edges (a(i),a(j)) of the cycle, such that both $a(i) \in E(k)$ and $a(j) \in E(k)$ for some k. Then two possibilities exist:

1) all vertices of a set E (k) are physically adjacent (Fig. 9(c)). When the total circuit layout graph is planar, then every possible embedding will satisfy the requirements.

2) The vertices of the set E (k) are not physically adjacent (Fig.10 (d)). Then not every embedding satisfies the requirements.

Therefore, we are able to use logical equivalence of subcomponents if the sets of terminals of subcomponents that are equivalent are physically adjacent.

Fig. 10(c) shows the correct model that allows partial subcomponent assignment in function of the layout (for subcomponents Al and A2).

6. Graph Models for the External Connections.

When the order of these connections is predetermined, one can again use an oriented graph. All nets now have to be embedded in the interior region (as opposed to the exterior region for components.).

In some cases, a certain degree of freedom exists, allowing logical signals to be assigned to physical terminals in function of the layout. This property is similar to the logical equivalence of the terminals of a component, As for components, the condition

for being able to model the logical equivalence of a set of terminals is that they are physically adjacent.

7. Conclusions

The mathematical model presented in this paper, based on the concept of partially oriented graphs, allows the formulation of the circuit layout problem as an embedding problem of partially oriented graphs. All of the topological information is contained in the model itself and no special constraints have to be imposed upon the embedding algorithm.

Furthermore, the models derived here allow pin and gate assignment in function of an optimal layout under certain conditions.

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Figure captions.

Fig. 1 (a) Planar embedding of nets $\{1,3,4,5,6,8\}$ and $\{2,7\}$

(b) Embedding of net $\{1,3,4,5,6,8\}$ creating a topological obstruction.

Fig. 2 (a) Non-planar circuit.

(b) Planar model for the circuit of Fig. 2(a).

(c) Planar circuit.

(d) Non-planar model for the circuit of Fig. 2(c).

Fig. 3 Physical equivalence of the terminals of an IC transistor.

Fig. 4 A 3-3-3 AND-OR-INVERT gate as an example of subcomponent equivalence.

Fig. 5 (a) Partially oriented graph, modelling the circular ordering of the terminals.

(b) Partially oriented graph modelling physical equivalence.

(c) Graph G' for verifying the possiblity of modelling physical equivalence of terminals.

Fig. 6 (a) Non-planar layout as a result of a priori pin assignment (terminals 3b and 3e physically equivalent).

(b) Planar layout obtained by performing pin assignment in function of the layout.

Fig. 7 (a) Circuit with logically equivalent sets A and B.

(b) After contracting the sets A and B.

(c) Correct oriented graph model.

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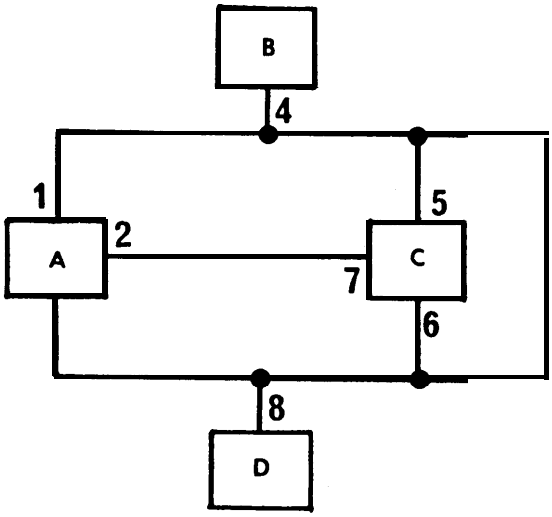
Fig. 9 Derivation of a model for subcomponent equivalence when equivalent subcomponents are physically adjacent.

Fig.10 Derivation of a model for subcomponent equivalence when not all equivalent subcomponents are not physically adjacent.



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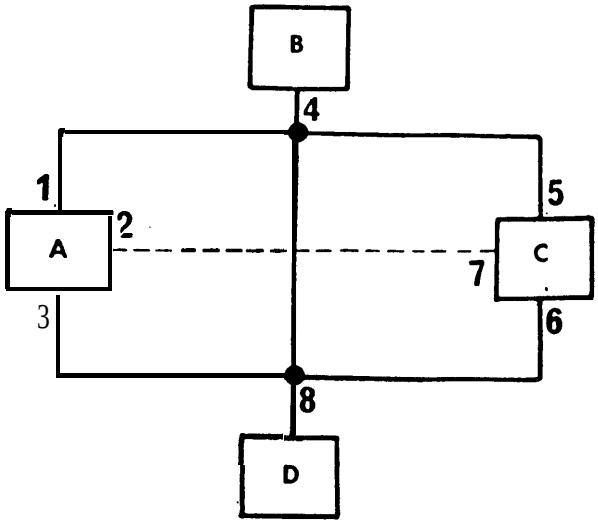

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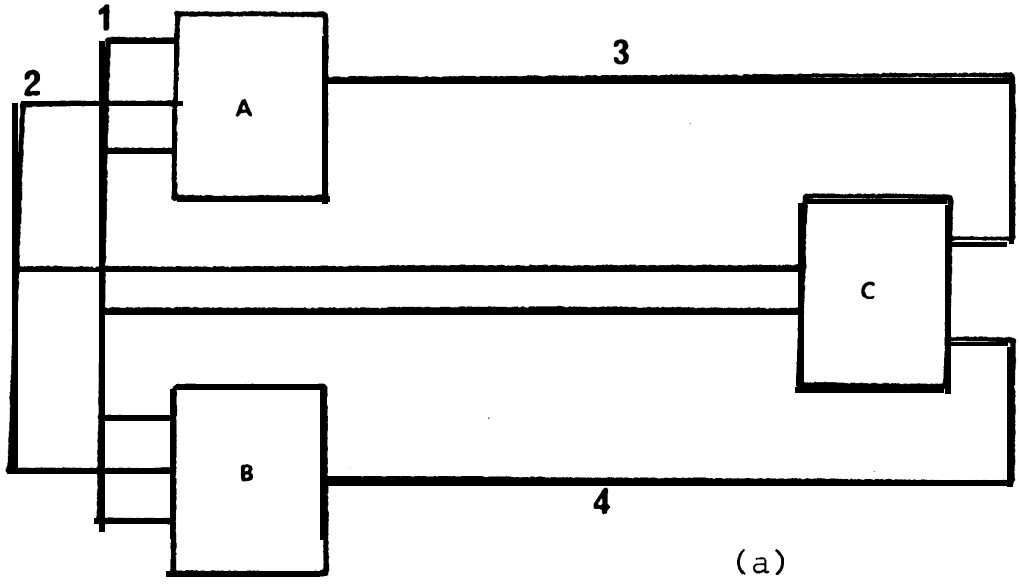

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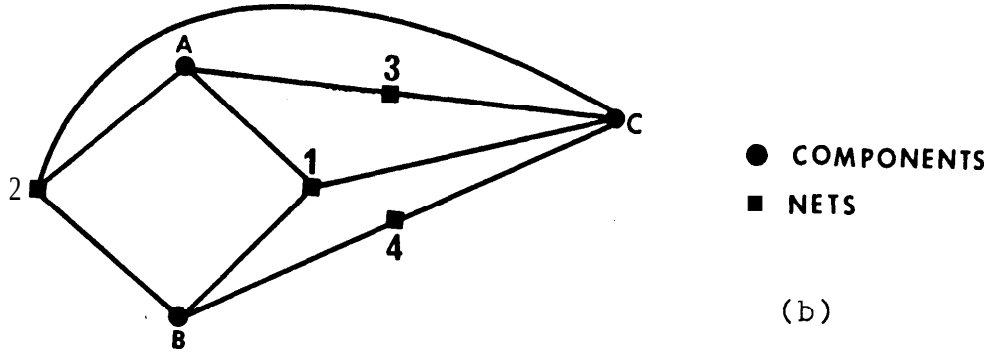

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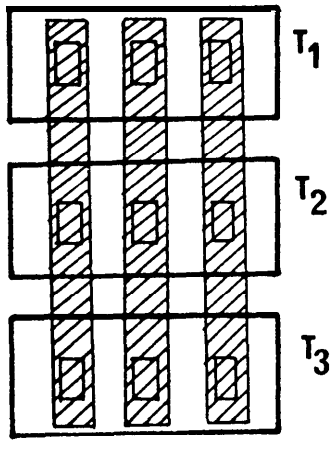

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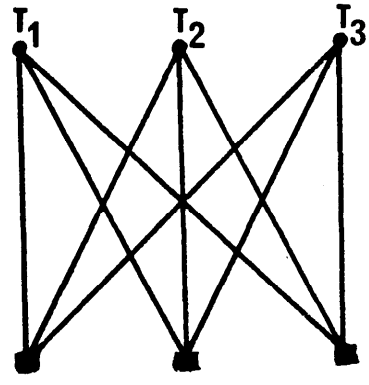

(d)

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(c) Planar circuit.

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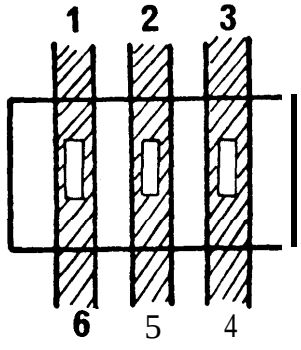

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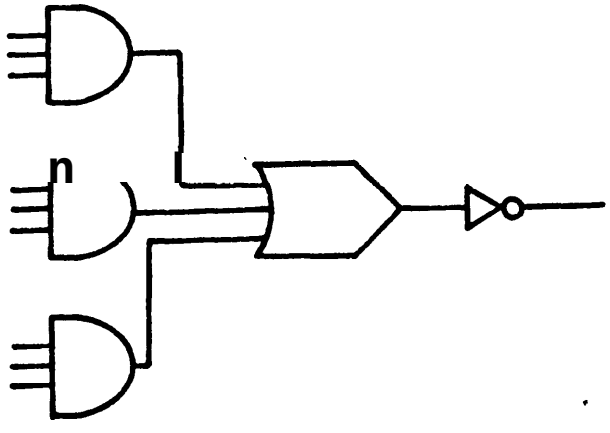

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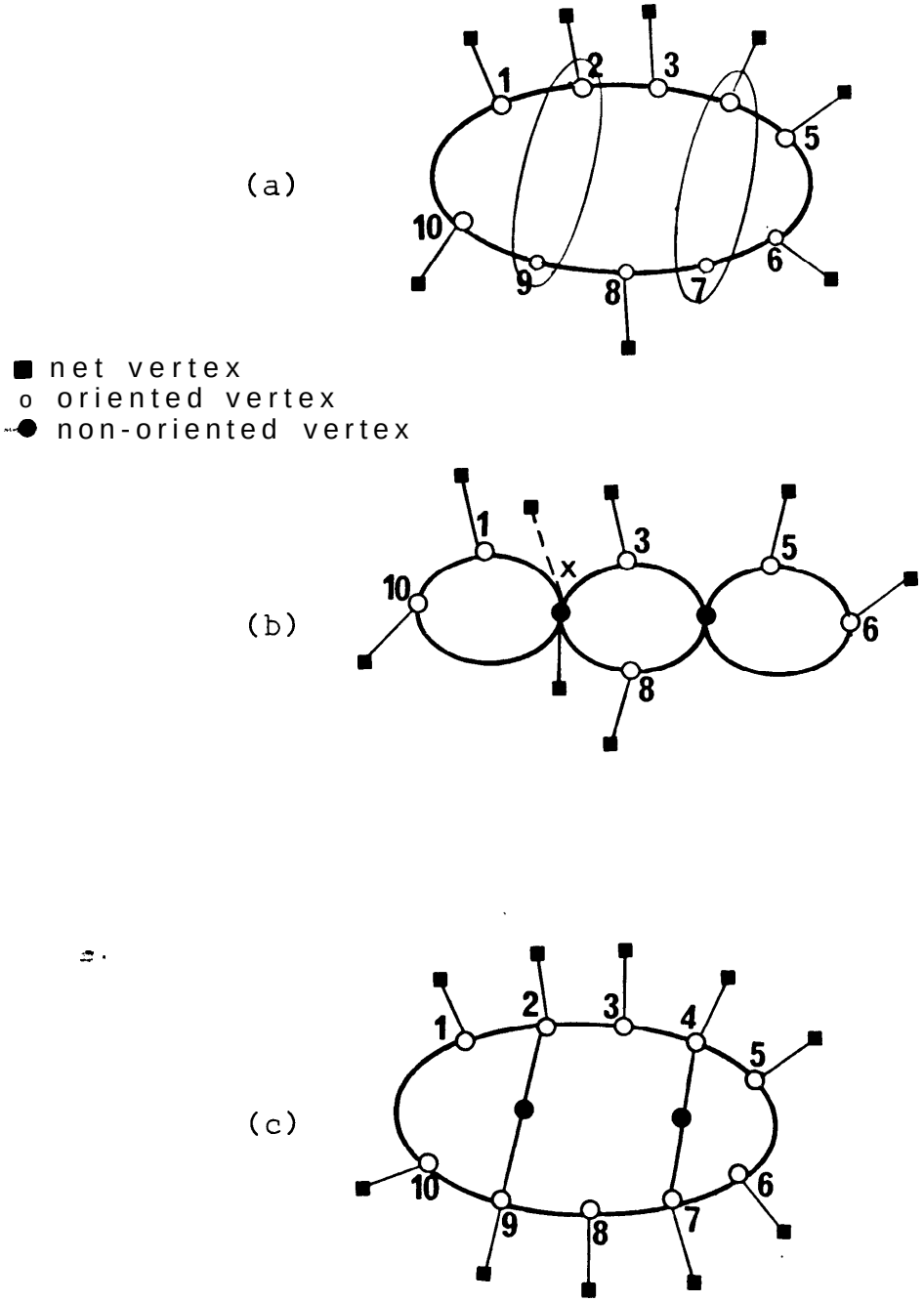

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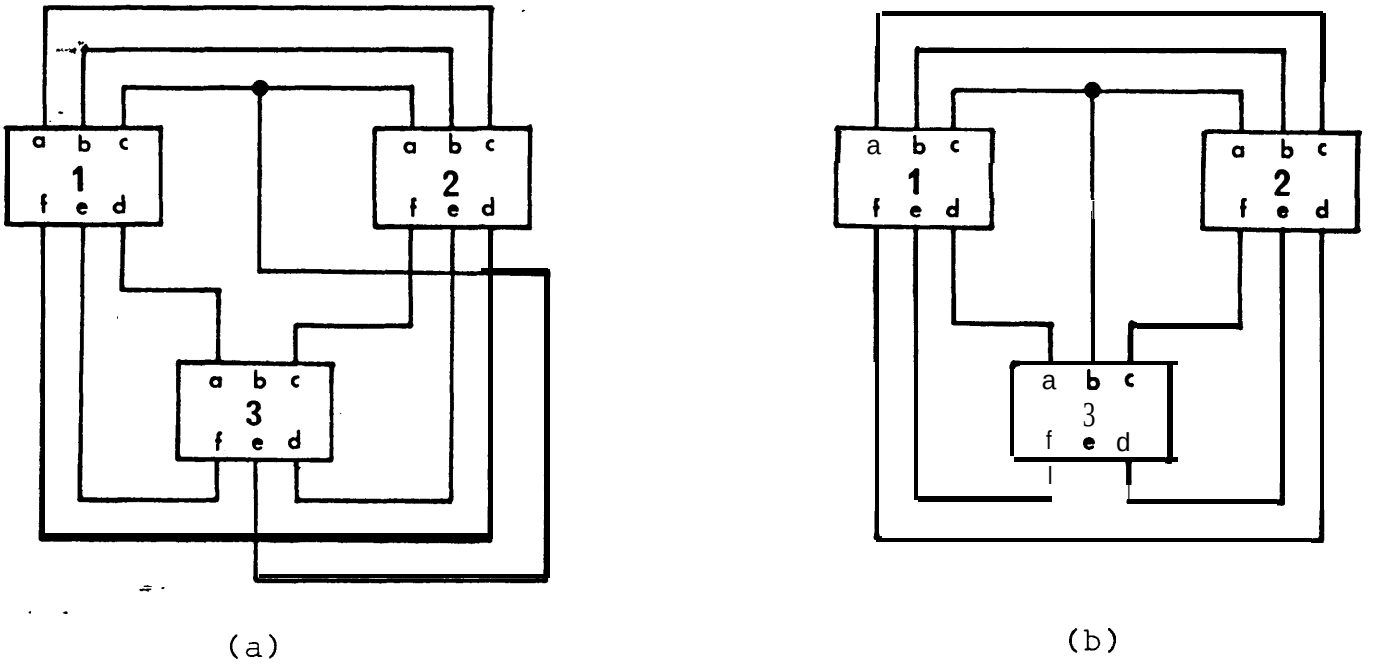

(a) (b)

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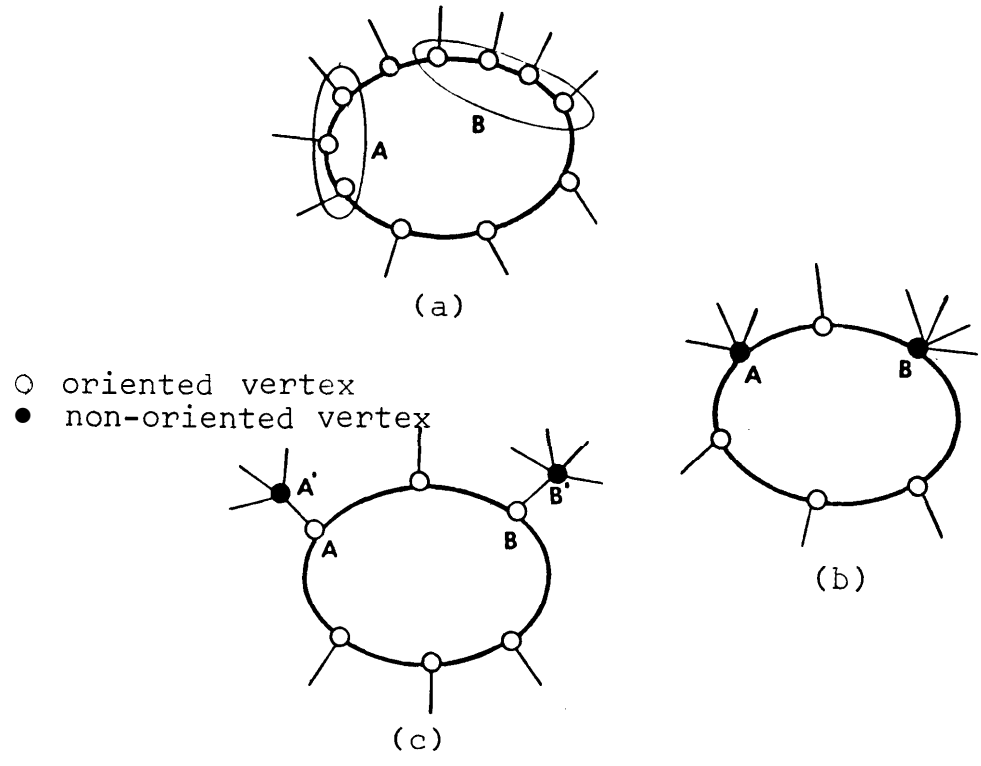

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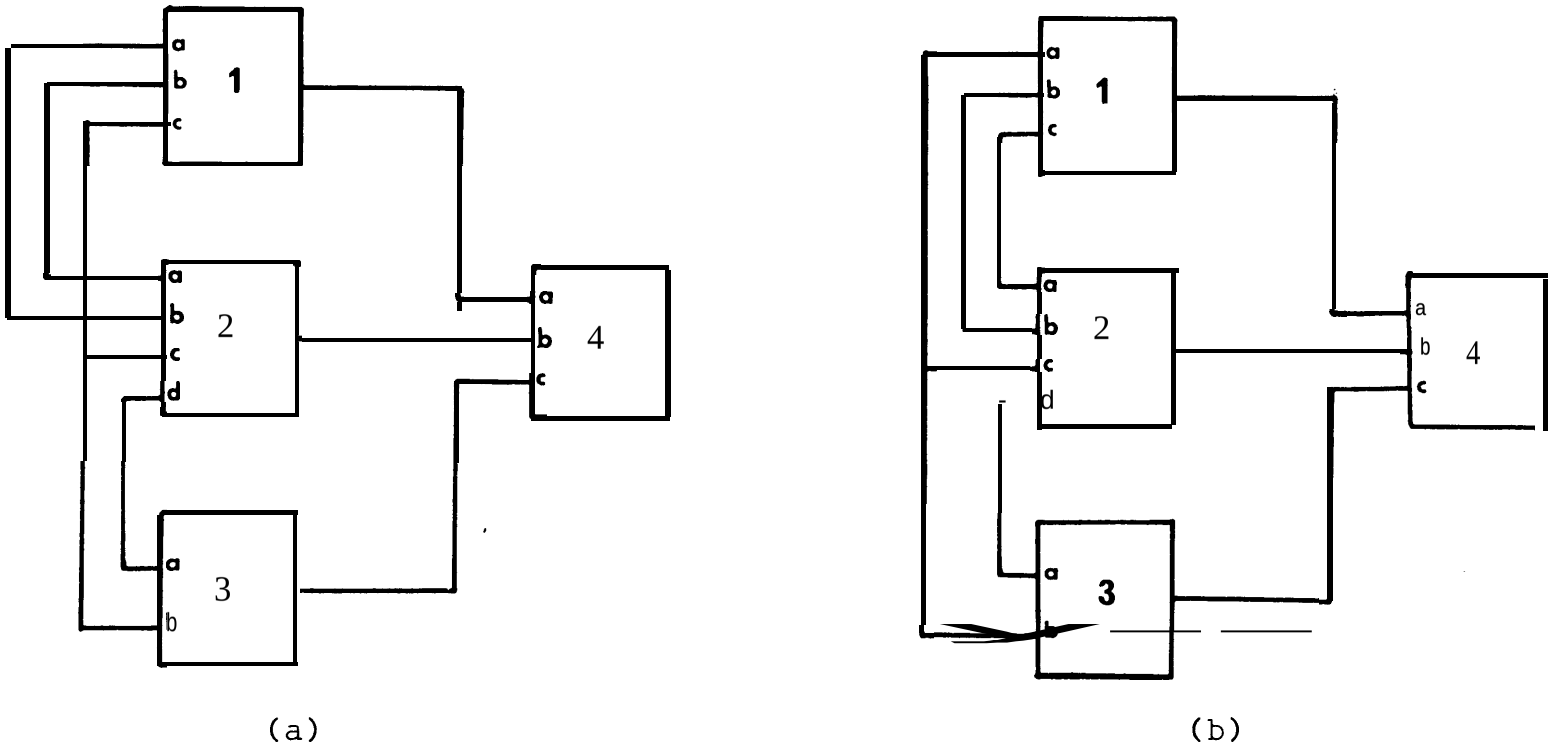

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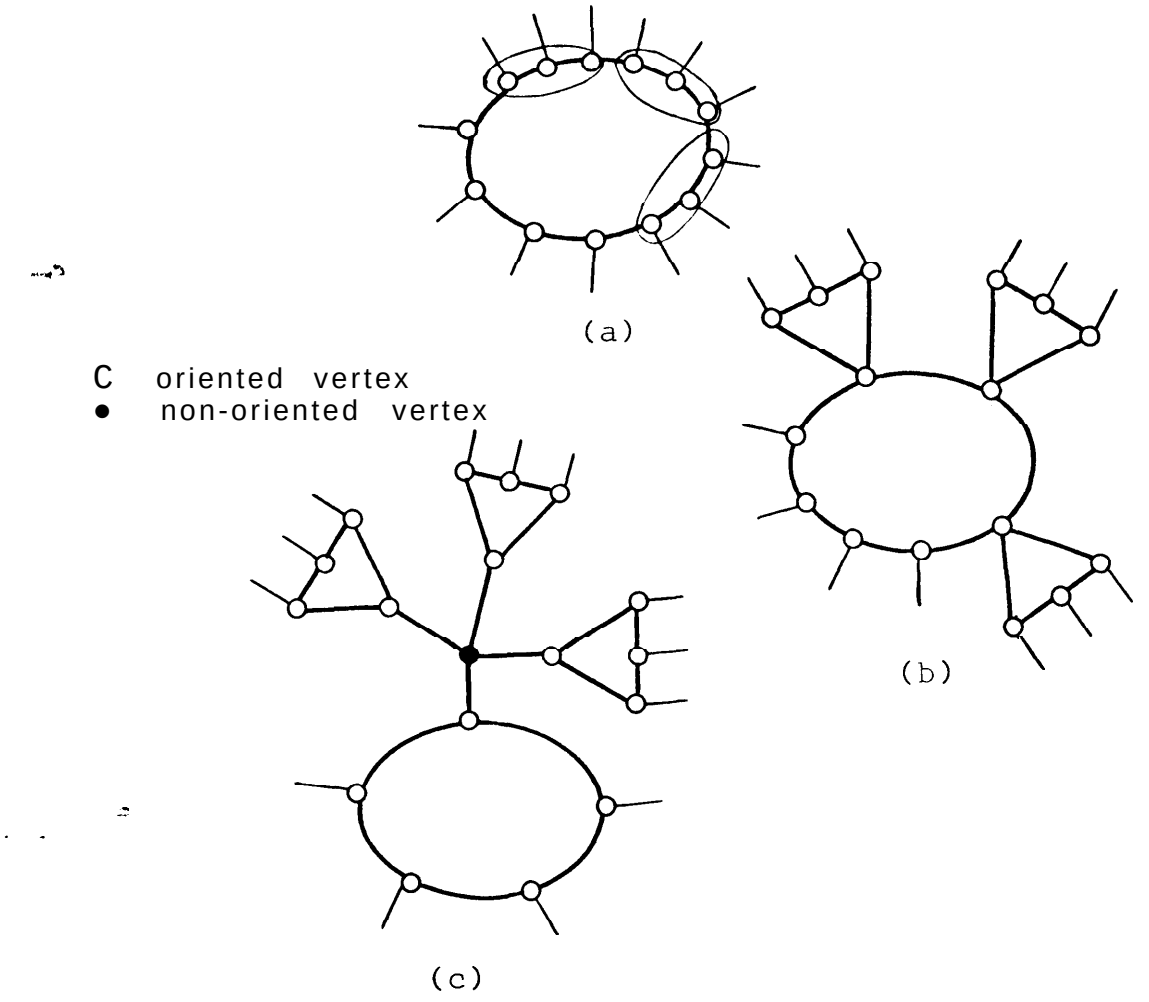

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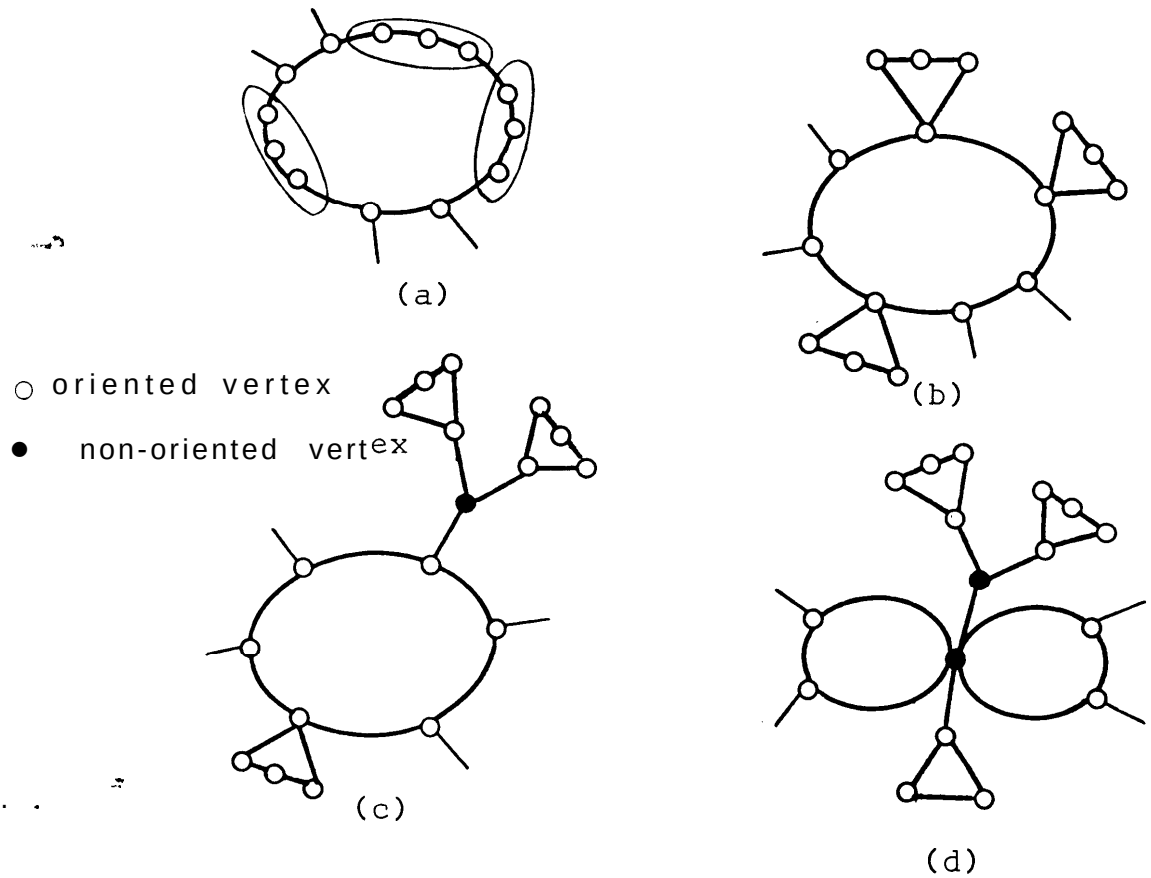

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