Asynchronous Serial Interface for Connecting a PDP-11 to the ARPANET (BBN 1822)

by

Ronald C. Crane

July 1976

Technical Report No. 116

This research was supported by the Defense Advanced Research Projects Agency under ARPA Order No. 2494, Contract No. MDA903-76C-0093.

DIGITAL SYSTEMS LABORATORY

STANFORD ELECTRONICS LABORATORIES

STANFORD UNIVERSITY • STANFORD, CALIFORNIA

Asynchronous Serial Interface for Connecting a PDP-11 to the ARPANET (BBN 1822)

Technical Report No. 116

July 1976

Ronald C. Crane
Digital Systems Laboratory
Departments of Electrical Engineering and Computer Science
Stanford University
Stanford, California

ABSTRACT

This report describes an interface to permit the connection of any PDP-11 to either the Packet radio network or the ARPAnet. The interface connects to an IMP on one side, meeting the specifications published in BBN report number 1822, and to a 16 bit parallel interface (DRV-11 or DR11-C) as described in the DEC peripherals and interfacing handbook. The interface card itself is a double height board (5.2"x8.5") which can be plugged into any peripheral slot in a PDP-11 backplane. The interface card is connected to the parallel interface card via two cables with Berg 40 pin connectors (DEC H-856) and to the IMP via an Amphenol bayonet connector (48-10R-18-31S). All 3 cables and connectors are supplied with the I/O interface card. The parallel interface card (DEC DR11-C or DRV-11) together with the special I/O interface card described in this report comprise the 1822 interface. The report includes descriptions of the operation of circuits, programming, and diagnostics for the 1822 interface.

KEY WORDS

BBN 1822 INTERFACE, HOST-IMP INTERFACE, LSI-11, PDP-11, DRV-11, DR11-C PACKET-RADIO-HOST INTERFACE, ASYNCHRONOUS SERIAL INTERFACE, ARPANET

This research was supported by the Defense Advanced Research Projects Agency under ARPA Order No. 2494, Contract No. MDA903-76C-0093

Table of Contents

l.Q Introduction

This report describes an interface to permit the connection of any PDP-11 to either the Packet radio network or the ARPAnet. The interface connects to an IMP on one side, meeting the specifications published in BBN report number 1822, and to a 16 bit parallel interface (DRV-11 or DR11-C) as described in the DEC peripherals and interfacing handbook. The interface card itself is a double height board (5.2"x8.5") which can be plugged into any peripheral slot in a PDP-11 backplane. The interface card is connected to the parallel interface card via two cables with Berg 40 pin connectors (DEC H-856) and to the IMP via an Amphenol bayonet connector (48-10R-18-31S). All 3 cables and connectors are supplied with the I/O interface card. The parallel interface card (DEC DR11-C or DRV-11) together with the special I/O interface card described in this report comprise the 1822 interface.

Except for differences in handling the IMP power relay status, this interface reflects the current prototype as constructed by SRI. In the SRI unit, an interrupt is continuously generated when the IMP goes down. The interrupt generation can be stopped by disabling the receiver, after which it is necessary to poll the interface to see if the IMP comes back up. The interface described here generates one interrupt on each change of state of the IMP.

The following sections describe the operation of circuits, programming, and diagnostics for the 1822 interface.

1.1 Block Diagram

The block diagram shows the basic parts of the special I/O interface card and its connections to the parallel interface card and the IMP.

The parallel interface card performs interrupt control on the PDP-11 unibus. It has 3 addresses on the Unibus; the control and status register, the output register, and the input gate. The status register includes both the interrupt enable bits as well as the transmit and receive enable bits. The output register is a buffer whose contents change only when the interface is loaded (written into). The input gate does not contain a buffer. Its function is only to gate its input signal to the Unibus. Thus the data sections of the I/O card need only store data for the receiver, but not the transmitter. A block diagram and description of the parallel interface unit supplied by DEC are in the appendix.

In the following section, the reader is referred to the block diagram as well as the circuit and timing diagrams that follow.

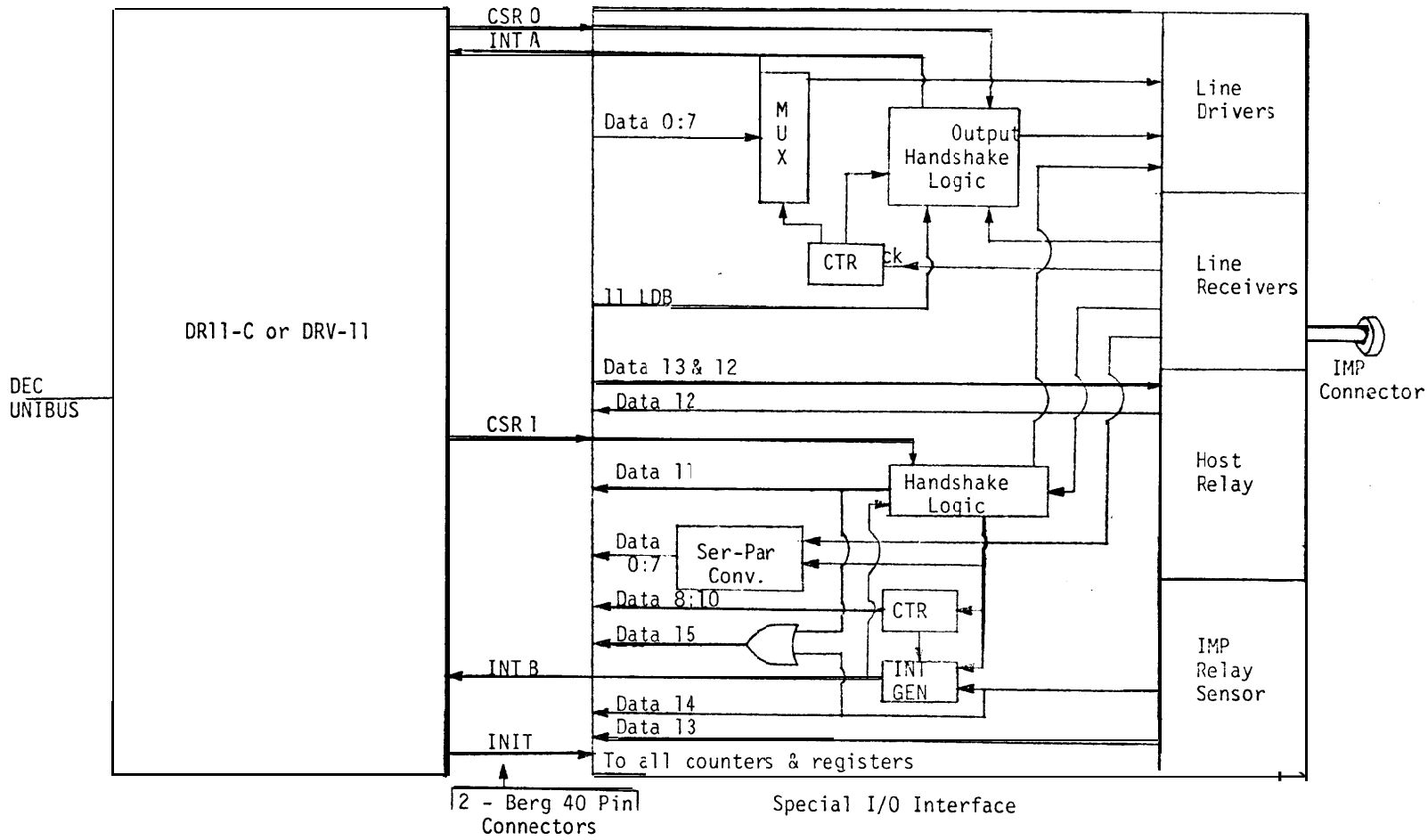


Figure 1
FUNCTIONAL BLOCK DIAGRAM

2.0 Transmit Section

The transmitter has two independent sections. One is the power relay and the other is the data section.

2.1 Host Power Relay

Bits 12 and 13 in the output register control the host power relay contacts. They are the R and S inputs to an R-S flip flop. Setting bit 12 closes the contacts, and setting bit 13 opens the contacts. If both bits are on, the contacts will be closed. If both bits are simultaneously cleared after both being set, the resulting contact position is indeterminate.

Last State		New State		Contact Status
Bit 13	Bit 12	Bit 13	Bit 12	
(any)		0	0	No change
(any)		0	1	Contacts closed
(any)		1	0	Contacts open
(any)		1	1	Contacts closed
1	1	0	0	Indeterminate
Initialize Pulse				Contacts open

Bits 12 and 13 need to be set only once, as can be seen from the table, since the state of the relay remains at its previous setting when bits 12 and 13 are both zero.

Since the transmit register cannot be used to read out the state of the relay, bit 13 of the receive register is used for that purpose. Bit 13 is a 1 if the contacts are open, and 0 if they are closed.

Bit 13 of INBUF	Contact position	
0	CLOSED	(Host power on)
1	OPEN	(Host power off)

The relay used is a Magnecraft W10Ø7-DIP-1 reed relay. Magnecraft claims the contact bounce is less than 500 microseconds. Therefore to be safe, no data should be transmitted until 1 millisecond after the relay is closed. This means that bit 12 of the transmit register (OUTBUF) must be set before transmit enable is 'set to prevent the interface from transmitting a byte when the power bit is set.

2.2 Data Section

The data section of the transmitter is an 8 bit parallel to serial converter implemented with a multiplexer. The 8 bit data byte and control information are supplied by the DR11-C whose output buffer holds these values until they are replaced by new data and control information.

2.2.1 Data Path

The actual parallel to serial conversion is done by an 8 line multiplexer (74152), which selects bits 7 to 0 of the output buffer and directly feeds the output driver. The bit selection is done by the low order 3 bits of a 4 bit binary counter (74193). The counter starts at zero and is advanced one count each time the RFNHB (Ready for Next Host Bit) line makes a high to low transition. On the 8th count the high order bit becomes a 1 and is used to inhibit further counting and also to generate a transmit interrupt request.

2.2.2 Handshaking Procedure

When the RFNHB line goes high, and transmit enable is a 1 (enabled), the TYHB (There's Your Host Bit) line goes high indicating availability of a data bit. RFNHB eventually goes low indicating acceptance of data. This triggers the 74123 pulse generator generating a pulse T4 seconds long (nominally 1 microsecond). The leading edge of the pulse advances the counter. The TYHB line is held low for at least the duration of the pulse, and possibly longer if the RFNHB line remains low for longer than the pulse duration. Using the pulse generator provides a straightforward method of meeting the minimum pulse width requirements for the 2-Way handshake. This is useful when operating over long cables. For systems using only a 4-Way handshake, a simple time delay would suffice as long as it is long enough to allow the counter and multiplexer to settle after being advanced (See transmit timing diagram for details).

2.2.3 Last Host Data Bit (LHDB) Signal

The LHDB signal is asserted if the Last Byte signal is present (bit 11 in OUTBUF is a 1) and the counter is selecting the last bit of the byte to be transmitted. The timing for this signal coincides with the timing for the data signal.

2.2.4 Transmit Enable

The transmit enable signal is used to gate out the interrupt request signal as well as to hold off data transmission while it is low. When the transmit enable signal is returned to the "1" (enabled) state, the transmitter waits for new data to be loaded into the output register (OUTBUF) before starting transmission. This means that the transmit enable line cannot be used to turn the transmitter on and off in the middle of a byte since the remainder of the byte would never be transmitted.

2.2.5 Initialize Pulse

The initialize pulse resets the counter to zero and opens the host power relay contacts. It also clears the registers in the DRV-11, thus clearing the transmit enable signal.

2.2.6 Load Pulse

The load pulse resets the counter and holds the TYHB line low for the duration of the load pulse (nominally 300 nano-seconds). If it is the first load pulse after the transmit enable line has been raised (=1), it also clears the hold-off flip-flop. The hold-off flip flop prevents handshaking from occurring until the first load pulse after the transmit enable line goes high.

2.2.7 Interrupt Request

A transmit interrupt can occur only after the last data bit has been received by the IMP and both of the following conditions have been met.

XMT enable is set	(=1)	Bit Ø in DRCSR
XMT interrupt enable is set	(=1)	Bit 6 in DRCSR

If one wishes only to poll the interface, only the XMT enable needs to be set. Bit 7 of the status register (DRCSR) indicates the state of the INT A line. If an interrupt has been requested, bit 7 will be a one. If bit 6 is also set, an interrupt will actually occur.

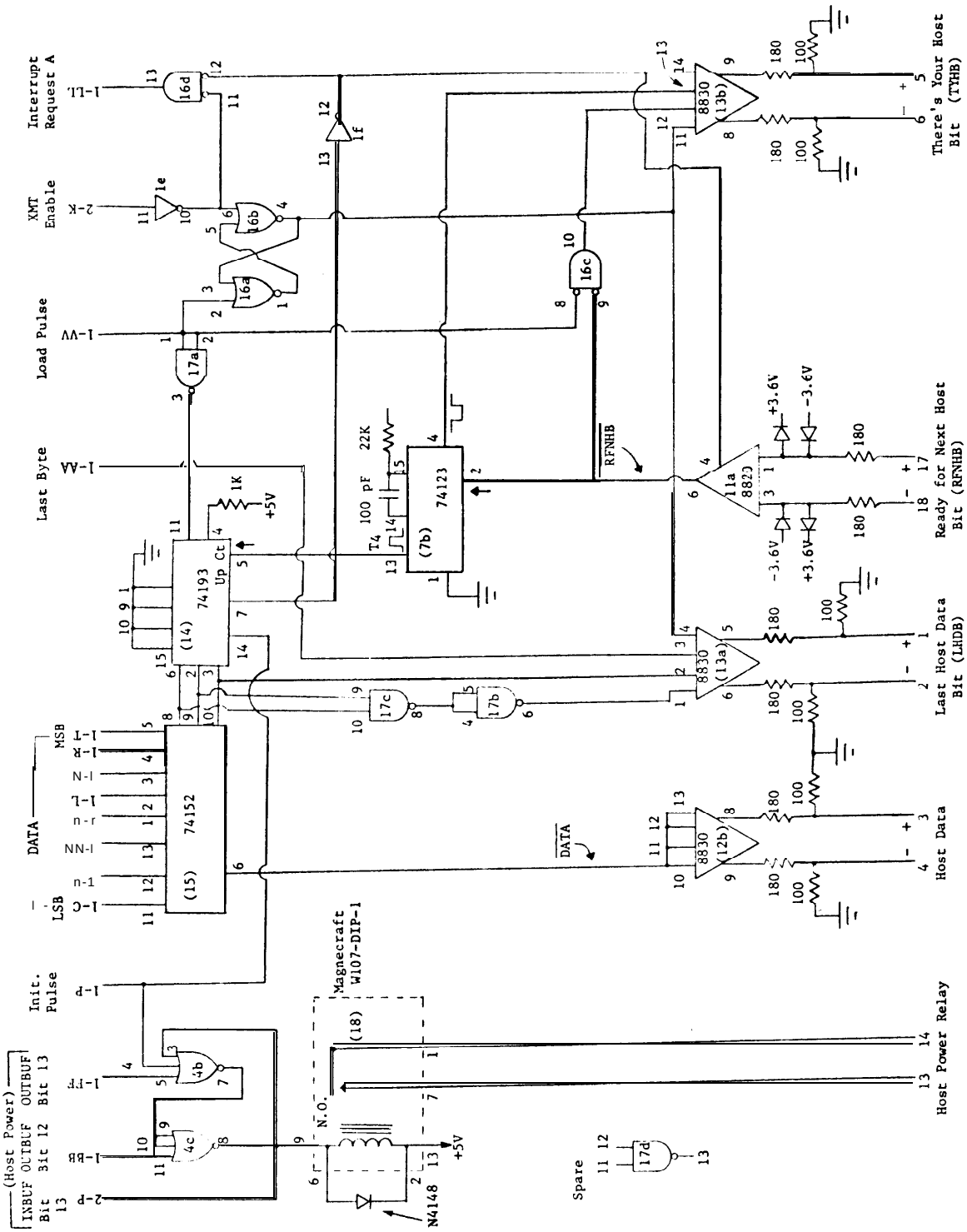
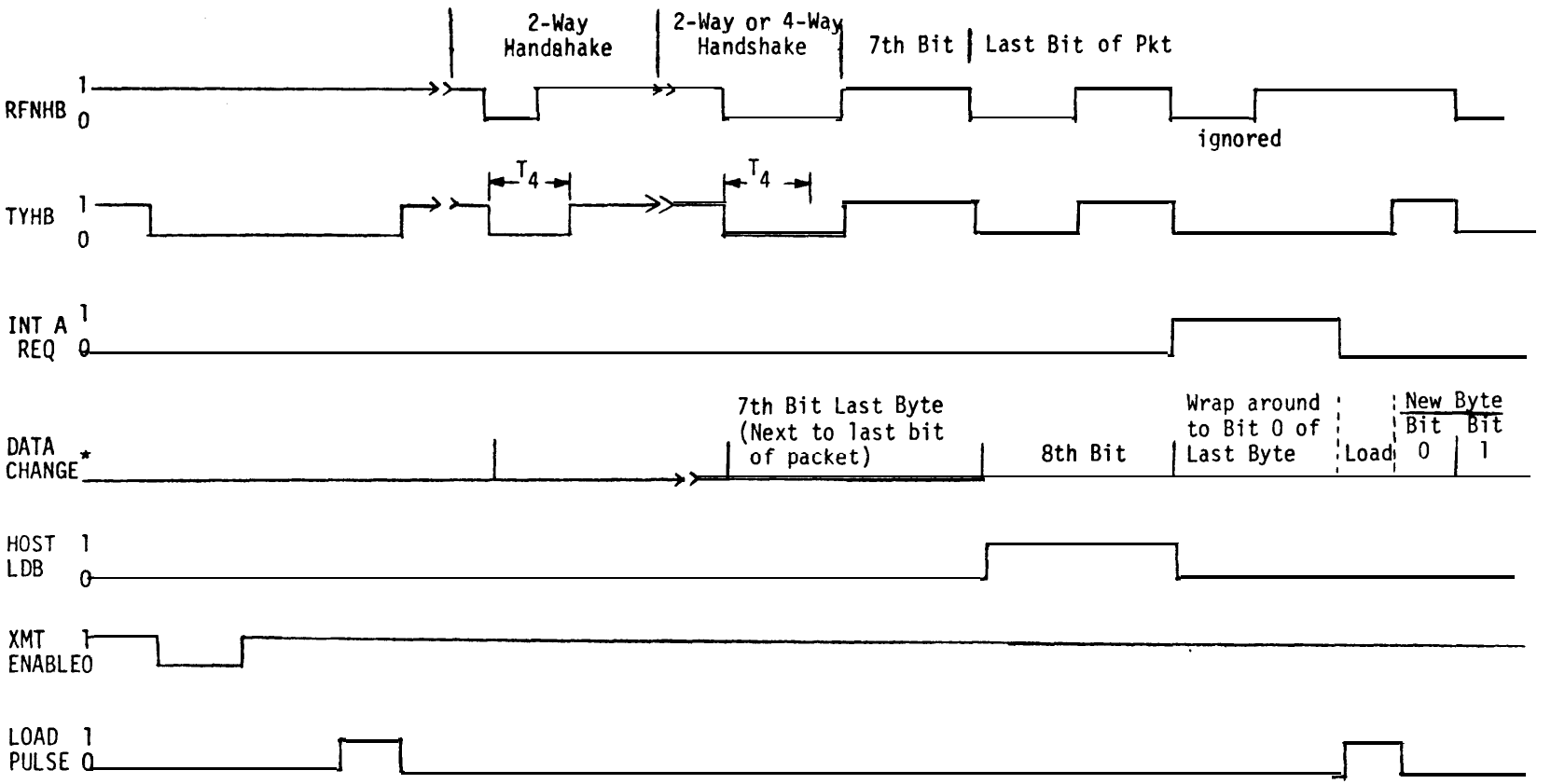


Figure 2 - Transmit Logic



* Vertical bar indicates transition

Nomenclature

↑ **Next** to an input lead indicates the device is clocked or triggered by a low to high level transition.

↓ **Next** to an input lead indicates the device is clocked or triggered by a high to low level transition.

⊓ A positive pulse appears on this lead. The width of the pulse may be indicated as well.

⊔ A negative pulse appears on this lead. The width of the pulse may be indicated as well.

▨ On timing diagram. Signal is irrelevant. Input can be either 0 or 1.

→≫ **Discontinuous** in time: timing sequences separated by a break may not follow each other in normal operation.

Figure 3
TRANSMIT TIMING

3.0 Receive Section

The receive section supplies one byte of data along with control information. The receiver is divided into two parts. One part senses the status of the IMP power relay contacts and the otner part performs the handshaking and serial to parallel conversion.

3.1 IMP Power Sensing

The IMP power relay contacts ground the filtered input to the inverter. The 39 ohm resistor, 5 microfarad capacitor and the 1ØK resistor provide some debouncing of the relay contacts. This supplies a signal through the inverters directly to the DRV-11 (bit 12). The high to low and low to high transitons generate a pulse via the EXCLUSIVE-OR gate and time delay which sets the power interrupt flip flop. See figure 4 illustratin g the EXCLUSIVE-OH pulse generator. An interrupt request is generated if the receive enable bit is set in the DRCSR (bit 1). An interrupt will actually occur if bit 5 is also set. These actions will occur independent of actions in the data section of the receiver. Bit 14 (=1) indicates that the interrupt was initiated by the INP power relay (IMP recently down) and bit 12 indicates the current status of the IMP relay.

3.2 Data Section

The data path in this section is from the line receiver directly to the serial-in, parallel-out shirt register (74164). The data is strobed into the shift register T1 sec. after the TYIB signal is asserted (=1). The time delay T1 allows deskewing of the signals on the TYIB line and the data and LDB lines. This time delay can be varied by changing the timing capacitor. After the data is strobed into the register, the RFNIB line is dropped (=Ø). It is held down for a minimum period of T2 sec. and possibly longer if the TYIB line has not dropped when T2 has elapsed. The RFNIB line will not go high again until the TYIB line is dropped. This meets the requirement of tne 4-Way handshaking procedure. The perioa T2 occuring after tile data is strobed into the register is to meet the minimum pulse width requirements when using the 2-Way handshaking procedure on long cables. The pulse width requirement at the IMP end of the cable can also be met by changing the appropriate timing capacitor on the interface card.

3.2.1 Interrupt Requests

An interrupt request can be generated only if the Receive enable line is high (DRCSR bit 1 is 1) and one of the following is true:

a) 8 bits have been received since the last interrupt as counted by the 74193 counter.
b) The Last Data Bit (LDB) flip flop has been set by receipt of an LDB signal.
c) The power status flip flop has been set due to a change in the status of the IMP power relay contacts. (Connecting and disconnecting the cable will have the same effect.)

3.2.2 Initialize and Read Pulses

Both the read and the initialize pulses produce a pulse on the clear line in the interface. The initialize pulse is inverted and fed directly to the clear line. The trailing edge of the read pulse indicates that the data has been read from the register. The pulse generator T3 generates a 1 microsecond pulse AFTER the trailing edge of the read pulse. When the clear line is lowered (=Ø), the register, flip-flops, and counter are cleared. T2 pulse generation is inhibited and the TYIB input signal is held low for the duration of a clear pulse.

3.2.3 Bit 15 Output

Bit 15 is the OR value of bit 14 (IMP recently down) and bit 11, the LIDB bit in the receive register. It is "1" only if the last bit of a packet has been received (the only time the LIDB line is asserted) or the the IMP has lost and/or regained power (its relay contacts changed position).

3.2.4 Data

The data bits appear in the low order byte of the receive register (bits Ø-7). The most significant bit (MSB) or bit 7 is the first bit received from the line and the least significant bit (LSB) or bit Ø is most recently received bit.

3.2.5 Bit Count

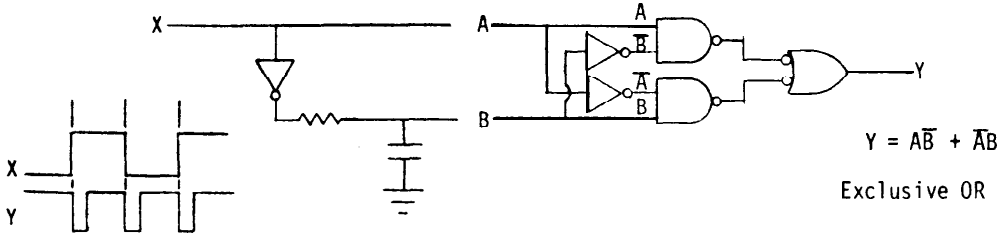
The three bits (8,9,1Ø) indicate how many bits have been received since the last interrupt. If a number other than Ø appears in these three bits, a full byte has not been received. The bits are a binary number indicating how many bits have been shifted into the register. The data bits are shifted into the low order byte starting at bit 0 and moving toward bit 7. Thus, the MSB starts at bit 0 and moves toward bit 7, its final destination. If the bit positions

were numbered 1 to 8 (LSB to MSB) instead of 0 to 7, then the bit count (10,9,8) is the position of the MSB. 000 means the MSB has reached its final destination.

3.2.6 Receiver Timing

See the timing diagrams for the receiver in figure 6.

Exclusive OR Pulse Generator (on level transitions)



Truth Table

Inputs	A	0	0	1	1
	B	0	1	0	1
Output		0	1	1	0

IMP Power Relay Receiver Circuit Pulse Generator

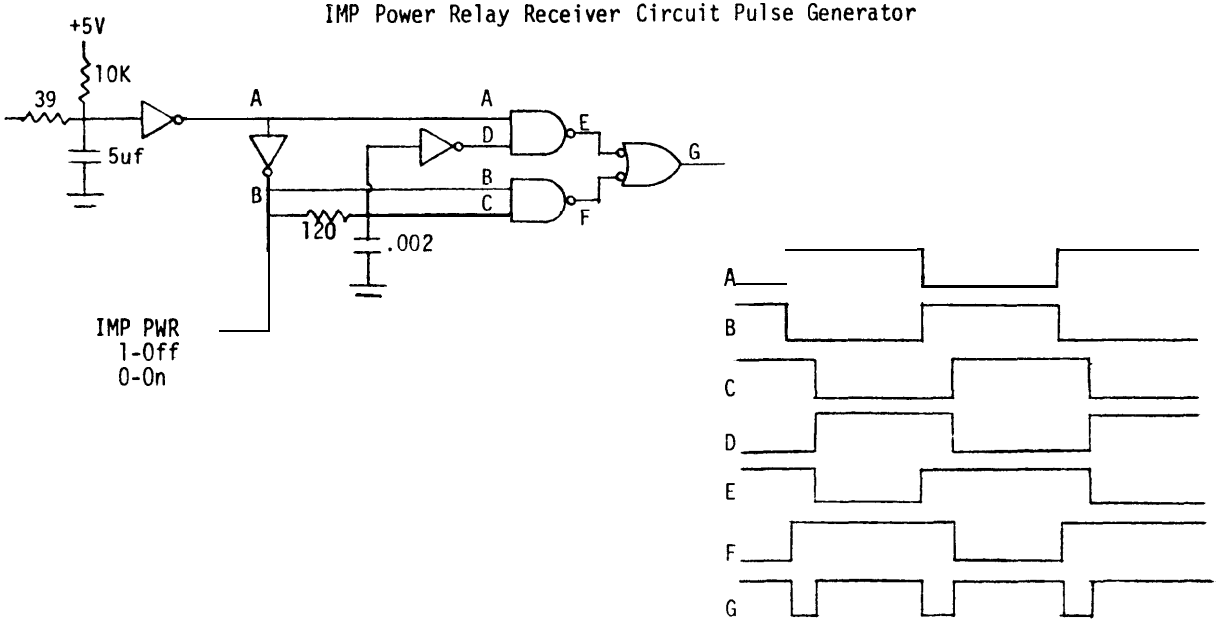


Figure 4 - EXCLUSIVE-OR Pulse Generator

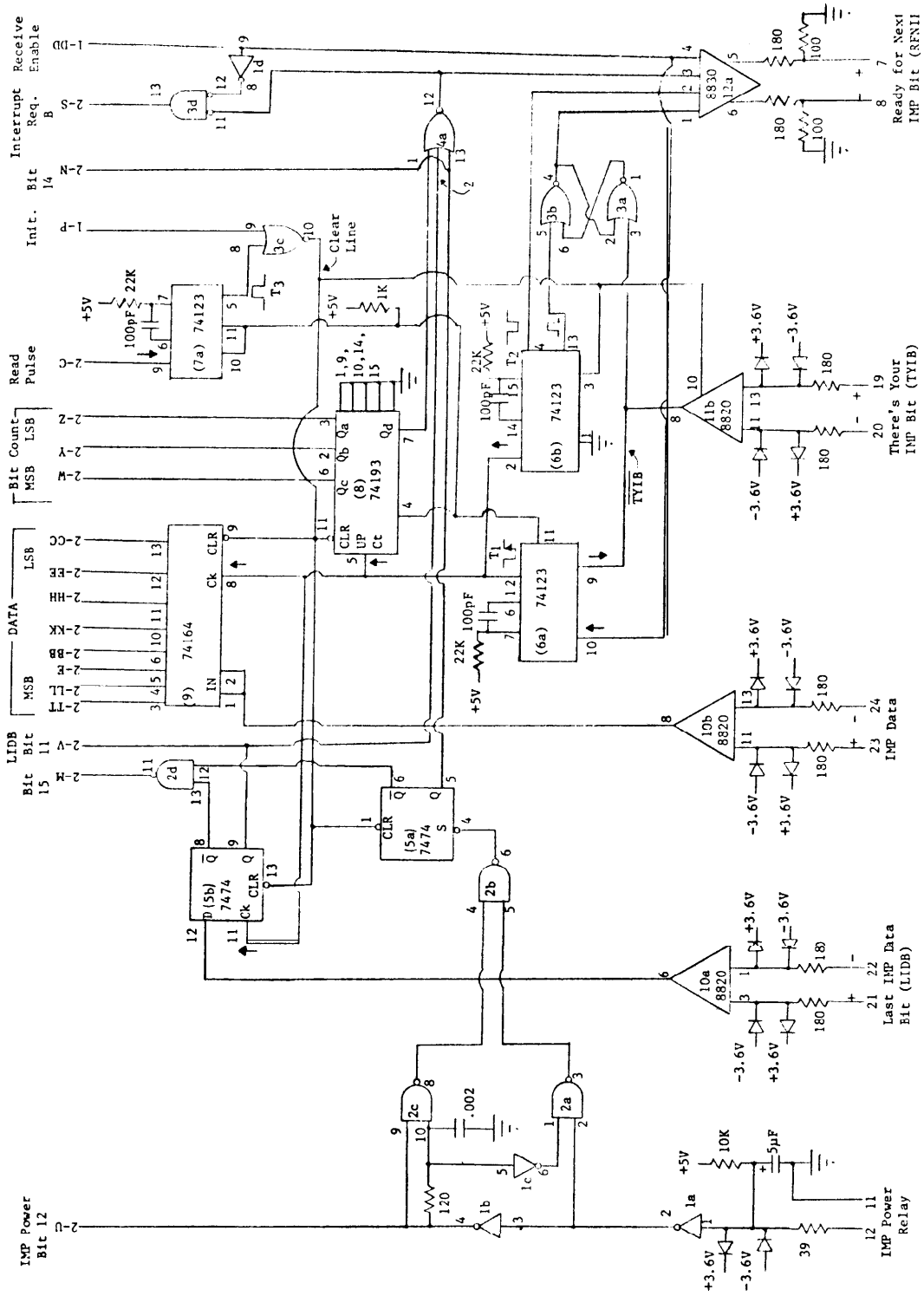
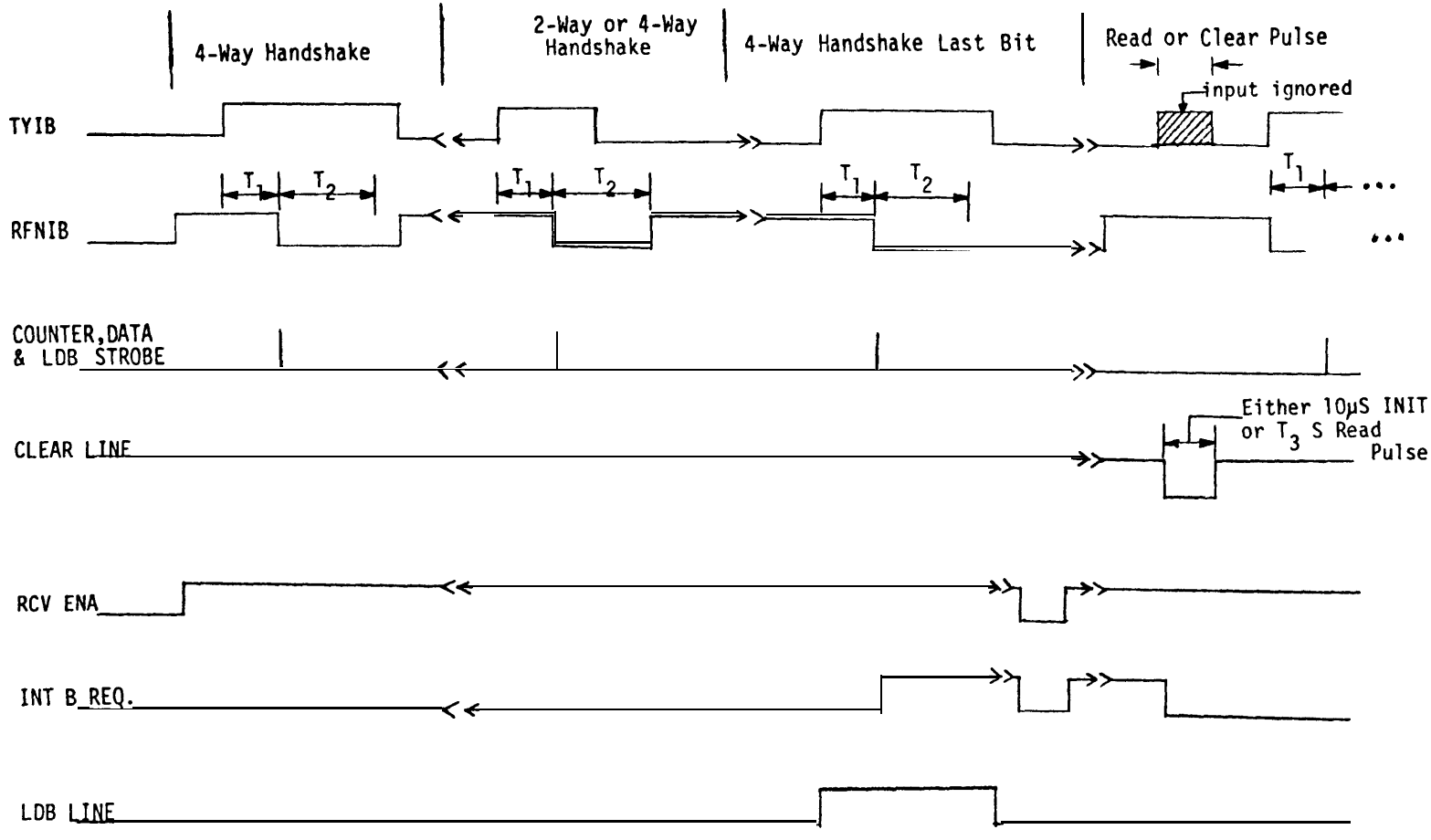


Figure 5 - Receive Logic



Nomenclature

- **Next** to an input lead indicates the device is clocked or triggered by a low to high level transition.
- **Next** to an input. lead indicates the device is clocked or triggered by a high to low level transition.
- A positive pulse appears on this lead. The width of the pulse may be indicated as well.
- A negative pulse appears on this lead. The width of the pulse may be indicated as well.
- On timing diagram. Signal is irrelevant. Input can be either 0 or 1.
- Discontinuous in time: timing sequences separated by a break may not follow each other in normal operation.

Figure 6
RECEIVE UNIT TIMING

4.0 Electrical Specifications

This section provides details on the power wiring for the board and data on the line drivers and receivers.

4.1 Line Drivers and Receivers (DM 8820 and DM 8830)

The line drivers are National DM 7830/8830 differential balanced drivers. The receivers are National DM 7820/8820 differential balanced receivers. Connection details are shown in the figure showing drivers and receivers. The receivers provide a high impedence (2.5K or 5K) termination of the line, with protective clamping at + and - 4 volts with respect to ground. When an input is out of the + or - 4 volt range, the input impedence from the out of range input to ground is 180 ohms. The maximum input voltage for any input lead should be held to + or - 10 volts with respect to ground. This is the dissipation limit of the protection circuit.

The outputs are balanced differential and provide a 1.2 volt differential voltage swing with a +.6 volt common mode voltage (both measured open circuit).

Logic State	Output A	Output B
Ø	0 v	+1.2 v
1	+1.2 v	Ø v

The output impedence is 130 ohms differential balanced with respect to ground (or 65 ohms to ground from each side).

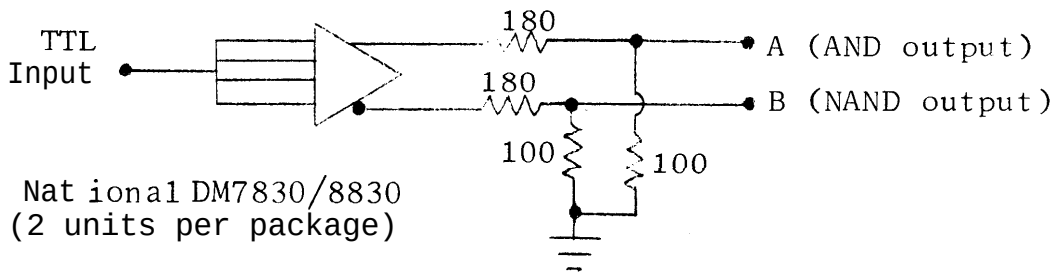
4.2 Power Distribution

The power distribution is shown in figure 8.

Figure 7

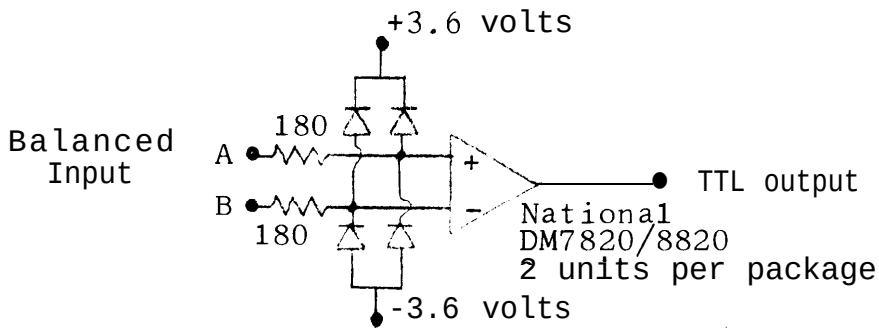
Line Drivers & Receivers
Electrical Specifications

I. Drivers: Differential Balanced Drivers (130 ohms balanced, 65 ohms each side to ground)

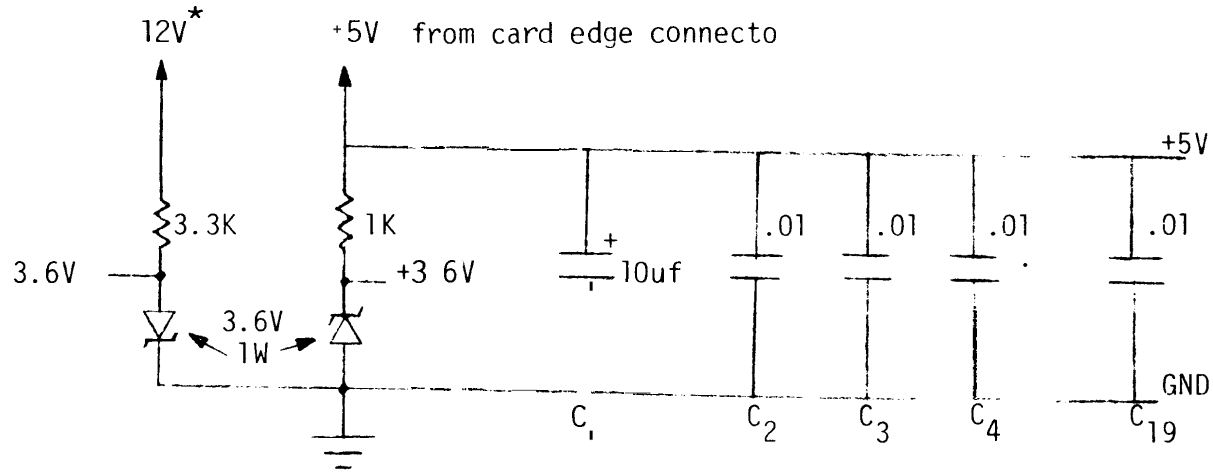


Input		outputs (volts)	
Logic	Voltage	A	B
0	0 v	0	1.2
1	3 v	1.2	0

II. Receivers Balanced Differential, NO termination



Diodes are 1N4148 or equiv.
Typical threshold voltage is 100 mV.
Non-inverting input resistance is 2.5K ohms to ground. (pins 3 & 11)
Inverting input resistance is 5K ohms to ground (pins 1 & 13).
Protection clamps input to receiver at + 4 volts. 180 ohm $\frac{1}{4}$ watt input resistor will fail with-sustained inputs above 10 volts.
The 7820 and 7830 operate over the military temperature range (-55°C to 125°C). The 8820 and 8830 operate over the commercial temperature range (0°C to 70°C).



* If -12V is not available, leave resistor unterminated.
The Zener will still protect against negative transients

Figure 8 POWER DISTRIBUTION

5.0 Changing Time Delays

The value of the time delays is linearly proportional to the value of the timing capacitor over reasonable values of time delay. Thus to change the time delays, the timing capacitors should be changed accordingly. All time delays shown are set to one microsecond.

6.0 Connectors

The I/O interface card makes 4 connections to the outside world.

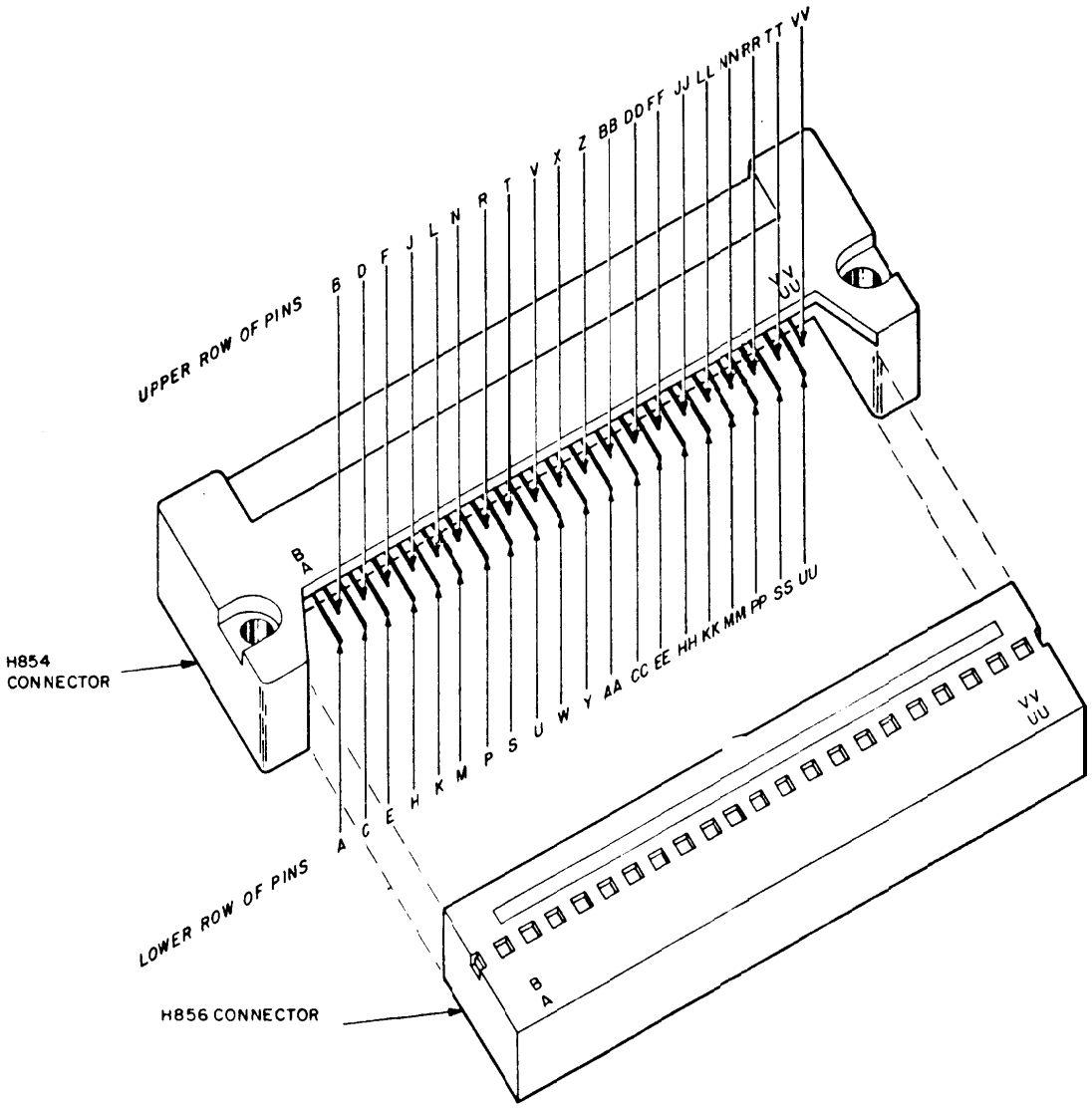
a) Edge connector on the card. DEC double height board. +5 volts and ground are used. Current consumption is about 600 mA.

b) Berg 40 pin connectors (2), one for input and one for output to parallel interface. They are labeled J1 and J2 corresponding to DEC nomenclature. (Pin numbers at the top of the schematics indicate the connector number and pin number. Connector 2, pin VV is 2-VV.) The connector number is DEC H-856

c) Amphenol 31 pin female bayonet connector. This is specified by the BBN 1822 report. The pin numbers for this connector are on the bottom of the schematics along with the signal name. The connector is Amphenol number 48-10R-18-31S.

6.1 Loopback Test Connector

Originate Pin No.	Destination Pin No.	Signal Name
1	21	+ LDB
2	22	- LDB
3	23	+ Data
4	24	- Data
5	19	+ TYB
6	20	- TYB
7	17	+ RFNB
8	18	- RFNB
11	13	Power Relay
12	14	Power Relay



J1 or J2 Connector Pin Locations

Figure 9 Berg Connector Pin Locations

7.0 Programming

The programmer has 3 registers to deal with in programming the interface: the status register, the input buffer, and output buffer.

7.1 Status Register

This register has 4 read/write enable bits, and 2 read only status bits. There are two enable bits, one each to allow operation of the transmitter and receiver. The two status bits indicate whether a receive interrupt request has occurred. An interrupt request can occur only if the respective transmitter or receiver has been enabled. An interrupt will actually occur if the appropriate interrupt enable bit (one for receive & one for transmit) has also been set.

7.2 Input and Output Buffers

Both the input and output buffers are divided into a data section (bits Ø:7) and a control section (bits 8:15). The user should not write into the transmit register or read from the receive register if they are in the process of transmitting or receiving a byte of data. Reading or writing into a register while it is in the process of transferring a byte may cause some bits to become lost and/or out of synchronization. This can be avoided by waiting until either an interrupt or interrupt request (as seen in the status register) is present before accessing the register.

7.3 Transmit (Output) Register

One byte of data will be transmitted each time this register is loaded if the transmit enable bit is set. Any old data will be cleared upon loading, independent of the state of transmit enable.

7.3.1 Data Section (Bits 0:7)

Bit 0 is least significant bit. Bit 7 is the most significant bit and is the first bit to be transmitted.

7.3.2 Control Section

Bit 11 (LHDB)- If this bit is set, the last host data bit line will go high during the transmission of the last data bit in the byte (bit 0).

Bit 12 - Host Power Relay Set- If this bit is set, the host power relay contacts will be closed indicating host is up. This bit need be set only once since the interface will latch the value. Either an initialize pulse or setting bit 13 will clear the latch. The latch will remain in the last state to which it was set. Bit 13 of the receive register contains the status of the latch.

Although the power latch can be set any time, it is recommended that the relay be turned on before the transmit enable bit is set in the status register. This prevents a data byte from being transmitted when the relay is turned on. It is important because the host must wait until the contacts have solidly closed before transmitting data which is approximately 1 mS for the relay used.

Bit 13 - Host power relay clear - Setting this bit clears the HOST power relay.

7.4.0 Receive Register

Reading the receive register clears the receive buffer making it ready for another byte. Thus program testing of control bits should be done after the contents of the receive register have been moved elsewhere. If the receiver wishes to suspend receipt of more data he can:

a) Not read the receive register.

b) Clear recieve enable after a receive interrupt and then read the receive buffer. In this case he has access to all data accepted by the interface and blocked data at the entry point to the interface.

c) Clear receive enable without waiting for an interrupt. In this case some bits may be lost. Setting receive enable will start the receiver again, but not necessarily where it left off.

7.4.1 Data (Bits 0:7)

Bit 0 is LSB and the last one received from the line. Bit 7 is MSB and the first one received from the line.

7.4.2 Control

Bits 8,9,10 - Point to last bit received in byte.

Bit 11 - (=1) Indicates last data bit line was asserted concurrently with receipt of the last data bit.

Bit 12 - IMP Power status. Indicates current status of the IMP power relay.

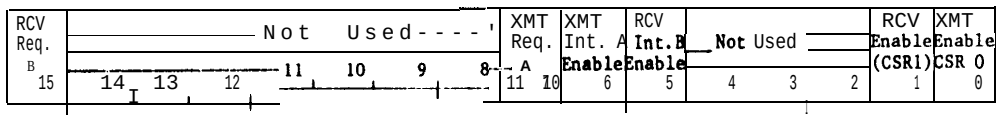
Bit 13 - Host power relay status. 0 - ON 1 - OFF

Bit 14 - Indicates the IMP has been down since the last interrupt was serviced. (i.e. the interrupt was generated by IMP changing status.) (see bit 12 for current status)

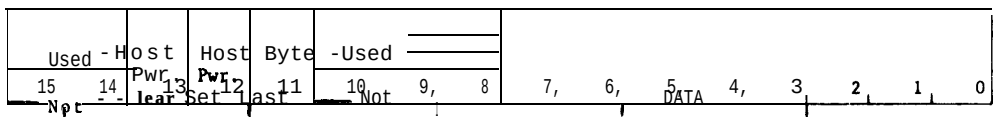
Bit 15 - Either bit 11 or 14 is a 1. This bit being set indicates the current interrupt requires special handling either because it is the last byte of a packet, or the IMP has been down.

Programming the 1822 Interface (with the DRV-11 or DR11-C)

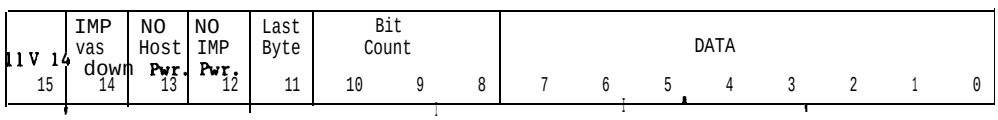
The bus address and interrupt vector locations shown are for the first DR11-C (DRV-11) in a system. If there is more than one DR11-C, or other devices competing for the same address area, the proper numbers may not be the ones shown. Check the appropriate system documentation and/or the hardware address jumpers on the DR11-C to be sure.



Control and Status Register - DRCSR 167770



Transmit Register - OUTBUF 167772



Receive Register - INBUF 167774

Control and Status Register DRCSR 167770

Bit	Function
Bit 15-	This bit indicates that the DRV-11 has received a request from the interface to generate an interrupt. If bit 5 of this register is set, an interrupt will occur. This bit is read only.
Bit 14-8	NOT USED
Bit 7	This bit indicates that the DRV-11 has received a request from the interface to generate a transmit interrupt. If bit 6 of the interface is set, an interrupt will occur. This bit is read only.
Bit 6	Transmit interrupt ENABLE- Setting this bit allows interrupts to be generated upon completion of transmission of each byte of data. This bit is read/write.
Bit 5	Receive interrupt ENABLE- Setting this bit allows interrupts to be generated upon receipt of each byte of data and/or a change in the status of the IMP power bit in the interface. This bit is read/write.
Bits 4-2	NOT USED
Bit 1	Receive enable- Setting this bit enables the receiver (by allowing the RFNB line to go high). The interface will then receive bits until either it is full, or it receives the last data bit (LDB) signal. At this point the interface stops and requests an interrupt. It will not accept any new bits until the present load of bits is read from INBUF. This bit is read/write.
Bit 0	Transmit enable-Setting this bit enables the transmitter (by allowing the TYB line to go high). The interface will transmit all bits which are loaded into OUTBUF after this bit is enabled. This bit is read/write.

Transmit Register OUTBUF 167772

All bits are read/write. Transmission of a byte is initiated each time OUTBUF is loaded, the transmitter is enabled (bit 0 of DRCSR is set).

Bit	Function
15-14	Not used
13	Setting this bit releases the Host relay contacts. This bit need be set only once, as the interface holds the information in a latch. Either bit 13 OR bit 12 should be set. NOT BOTH.
12	Host Power Set- This bit sets the Host relay contacts. As with bit 13, this bit need be set only once, since the interface holds the information in a latch. Either bit 13 or bit 12 should be set. NOT BOTH. No data should be sent until at least 1 millisecond after this bit is set to allow for relay contact bounce.
11	Last Data Byte- This bit causes the last data bit (LDB) line to go high concurrently with the transmission of the last bit of the byte. This is typically set with the last byte of a packet.
10,9,8	NOT USED (On the early unit, these bits indicated the last bit position to be transmitted within the byte.)
7-0	DATA (Bit 7 is the high order byte, and bit 0 is the low order byte.)

Receive Register INBUF 167774

The interface will receive bits until either it is full, or it receives the last IMP data bit (LIDB) signal. At this point the interface stops and requests an interrupt. It will not accept any new bits until the present load of bits is read from INBUF.

BIT	FUNCTION
15	Special conditon - If set, the byte of data just received requires special handling. (i.e. it is either the last byte of a packet, or there has been a change in the status of the IMP relay contacts (IMP recently down).
14	IMP just went down or IMP has been down and just came up Ø - No change in IMP status 1 - IMP has been down recently (see bit 12 for current status).
13	HOST POWER- Indicates the current status of the Host power relay as set or cleared by either bit 12 or 13 respectively in the transmit register OUTBUF. This bit should be interpreted as follows: Ø - HOST power relay contacts closed (ON) 1 - HOST power relay contacts open (OFF)
12	IMP POWER- Indicates the current status of the IMP power relay. The bit should be interpreted as follows: Ø - IMP power ON 1 - IMP power OFF (See bit 14 to determine if the interrupt was generated by the power circuit.)
11	LAST BYTE - If this bit is set, the data byte is the last one in a packet. Bits 8,9,10 should be checked to determine the position within the byte of the last bit transmitted.
10,9,8	Bit Count - The three bits (10,9,8) indicate how many bits have been received since the last interrupt. If a number other than Ø appears in these three bits, a full byte has not been received. The bits are a binary number indicating how many bits have been shifted into the register. The data bits are shifted into the low order byte starting at bit Ø and moving toward bit 7, its final destination. If the bit positions were numbered 1 to 8 (LSB to MSB) instead of 0 to 7, then the bit count (10,9,8) is the position of the MSB. 000 means the MSB has reached its final destination (position 8).
7-Ø	DATA - Bit 7 is the MSB of the data byte and is the first bit of the byte to be received from the IMP.

INTERRUPT VECTORS FOR THE INTERFACE

Transmit Interrupt Vector

Loc.	Contents
300	XMT =(PC)
302	200 =(PS)

Receive Interrupt vector

Loc.	Contents
304	RCV =(PC)
306	200 =(PS)

XMT- Address of transmit interrupt routine
RCV- Address of receive interrupt routine

8.0 Diagnostics

It is assumed that the DR11-C or DRV-11 is functional before these tests are attempted. If the above is not true, the programmer/user has no means of accessing the special I/O card. If in doubt, the DR11-C tests should be run first.

8.1 Packet Source/Sink

8.2 Scope Loop

8.1 Packet Source Sink Program

8.1.1 General

The packet source and sink program can be used to make the interface do handshaking for hardware and software checkout purposes.

The transmit part continuously loads the contents of 16 sequential memory locations into the transmit buffer. The low order byte is transmitted as data. Bit 11 of the high order byte may be set both as an end of packet indicator and also to test the LDB lines in the interface.

The receive or sink program circularly fills a 16 word area in memory with the contents of the receive register. The user may stop the program at any time to see the contents of the last 16 bytes received.

8.1.2 Running Source/Sink Program

A) Location 602 determines what the program does. It is loaded into the control and status register of the interface. It should be loaded with one of the following.

101 Transmit Only
42 Receive Only
143 Transmit & Receive

B) Locations 440 to 476 (octal) contain the transmit buffer. They should be filled with the data and control as the user wishes. Words from the buffer are successively loaded into the output buffer of the interface.

C) Load the program into memory using ODT or switch register. Alternately assemble the listing and load it from some storage device.

D) The program starts at location 600 (octal) after it is loaded.

8.1.3 Source/Sink Program

Memory location (octal)	Contents (octal)	Function
300	1000	\
302	200	I- Interrupt Vectors
304	700	|
306	200	/
400		\
|		|- Receive Buffer 16 words (8 received
		I bytes)
436		/
44Q		\
|		I- Transmit Buffer 16 words (8 transmitted
		I bytes)
476		/
600	12737	MOV C(loc 602),DRCSR
602	see table	101-Transmit 42-Receive 143-Both
604	167770	
606	127615	R5=440
610	440	
612	12704	R4=400
614	400	
616	12706	R6=2000
620	2000	
622	12537	MOV (R5)+,OUTBUF Start transmitter
624	167772	
626	777	BR 626 Wait loop
700	13724	MOV INBUF,(R4)+
702	167774	
704	22704	COMP #440,R4
706	440	
710	1002	BNE 716
712	12704	R4=400
714	400	
716	2	RTI
1000	12537	MOV (R5)+,OUTBUF
1002	167772	
1004	22705	COMP #500,R5
1006	500	
1010	1002	BNE 1016
1012	12705	R5=440
1014	440	
1016	2	RTI
16777Q		DRCSR
167772		OUTBUF
167774		INBUF

8.2 Scope Loop Program

8.2.1 Running Scope Loop Program

A) Load Source/Sink program in 8.1.3 .

B) Location 602 should be 143 (transmit & receive)

C) Locations 440 to 446 should be:

```
440   000000
442   000002
444   000200
446   004001
```

D) Change contents of location 1006 from 500 to 450 so transmitter loops after 4 bytes.

E) Start program at location 600 (octal).

8.2.2 Using Scope Loop

The loop program transmits two word packets. They are transmitted continuously. They are:

Word 1 000002 octal

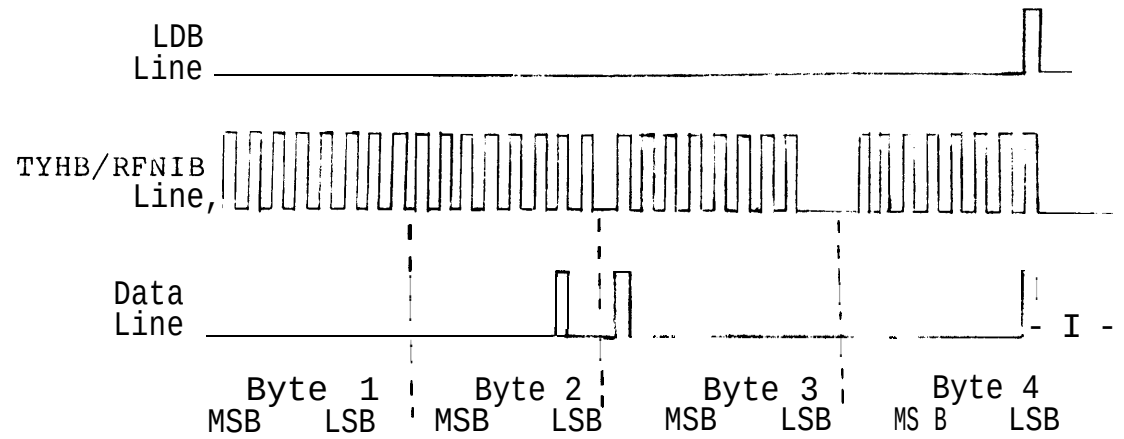
Word 2 100001 octal

The most significant bit (MSB) of each word is transmitted first. Thus, the bytes are sent as follows:

Memory Location	Byte No.	Octal MSB	Octal LSB	Binary MSB	Binary LSB	
440	1	000		00000000		
442	2	002		00000010		
444	3	200		10000000		
446	4	001		00000001		(LHDB asserted with LSB of byte 4)

The last host data bit (LHDB) line is asserted with the last bit (LSB) of the second word.

Scope Pattern for Test Program
(with loopback connector)



Appendix

GENERAL DEVICE INTERFACE, DR11-C

DESCRIPTION

The DR11-C is a general-purpose interface between the PDP-11 UNIBUS and a user's peripheral. The DR11-C provides the logic and buffer register necessary for program-controlled parallel transfers of 16-bit data between a PDP-11 System and an external device. The interface also includes status and control bits that may be controlled by either the program or the external device for command, monitoring, and interrupt functions.

The DR11-C interface consists of three functional sections: address selection logic, interrupt control logic, and device interface logic.

The address selection logic determines if the interface has been selected for use, which register is to be used, if a word or byte operation is to be performed, and what type of transfer (input or output) is to be performed.

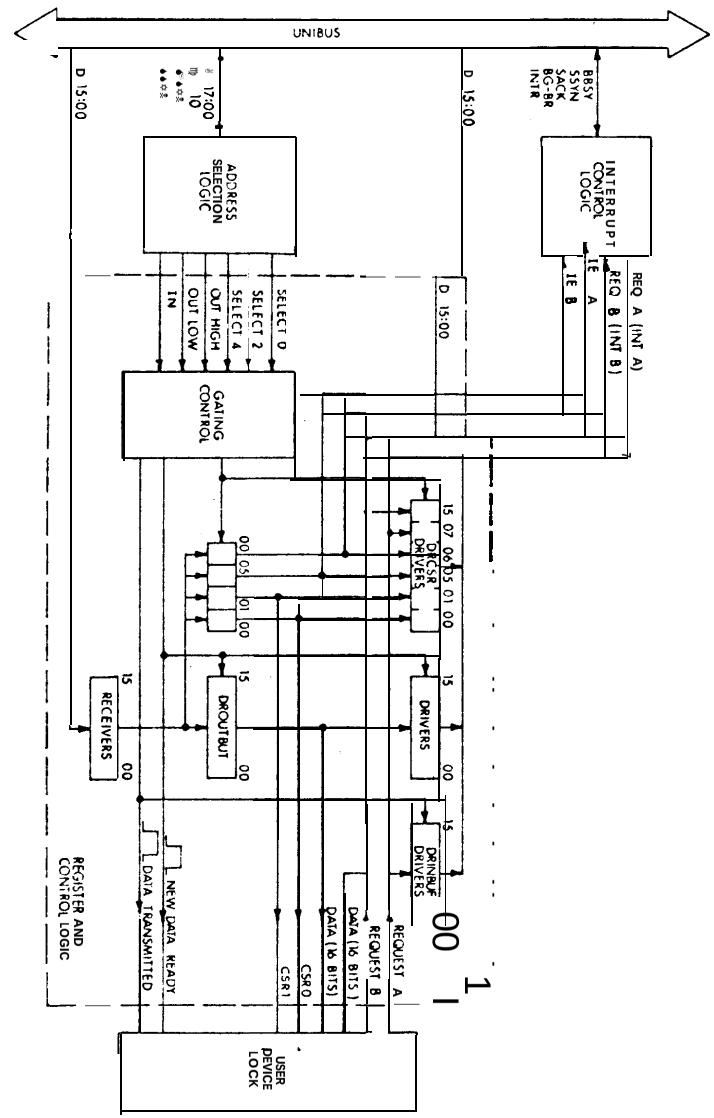
The interrupt control logic permits the interface to gain bus control and perform program interrupts to specific vector addresses. The interrupt enable bits are under program control; the interrupt bits are under control of the user's device.

The DR11-C interface logic consists of three registers: control and status, input buffer, and output buffer. Operation is initialized under program control by addressing the DR11-C to specify the register and the type of operation to be performed.

If an output operation is specified, information from the UNIBUS is stored in a 16-bit register. Once this register has been loaded under program control (e.g., MOV R0, OUTBUF), the outputs are available to the device until the register is loaded with new data from the bus. The register can also be read onto the bus. Upon transfer of data to the buffer register, a NEW DATA READY control signal is supplied to indicate to the user's device that data has been loaded by means of a DATO or DATOB bus cycle and is read by means of a DATI or DATIP bus cycle.

When an input operation is specified, the DR11-C provides 16 lines of input to UNIBUS transmitters. This permits data from the user's device to be read onto the bus. A control signal, DATA TRANSMITTED, informs the device that the input lines have been read. The input lines, which are not buffered, can be read by a DATI bus cycle (e.g., MOV INBUF, R0).

The control and status register provides six bits that can be used to control and monitor user functions. Two of these bits are interrupt enable (INT ENB) bits under control of the program. Two bits (REQ A and B) are under direct control of the user's device and can only be read by the program. These bits can be used either to initiate interrupt requests or to provide flags that can be monitored by the program. The remaining two bits (CSR0 and CSR1) are read/write bits that can be controlled by the program to provide command or monitoring functions. In the main-



DR11-C Interface, Block Diagram

tenance mode, they are also used to check operation of the interface.

A maintenance cable, which is supplied with the interface, permits checking of the DR11-C logic by loading the input buffer from the output buffer rather than from the user's device. Thus, a word from the bus is loaded into the output register and the same word appears when reading the input buffer, provided the interface is functioning properly.

The DR11-C can also be used as an interprocessor buffer (IPB) to allow two PDP-11 processors to transfer data between each other. In this case, one DR11-C is connected to each processor bus and the two DR11-Cs are cabled together, thereby permitting the two processors to communicate.

Physical Description

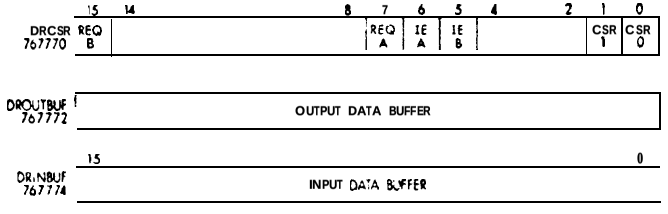
The DR11-C interface is packaged on a single quad module that can be plugged into a small peripheral slot (SPC).

The module has two Berg connectors for all user input/output signals. Two M971 connector boards, which are not supplied with each interface, can be used to bring all input/output lines to individual pins on a back panel via two H856 cables. Note that this cable is a "mirror image" rather than a straight one-to-one cable.

The following accessories are available for interfacing:

a. BC08R (Berg-to-Berg) flat cable. Available in lengths of 1, 6, 8, 10, 12, 20, and 25 feet. When ordering, the dash number indicates the desired cable length; e.g., BC08R-1 or BC08R-25.
b. M971 connector board. A single-height by 8-1/2 in. board that brings the signals from one Berg connector to the module fingers.
c. BC11K-25 cable. Consists of a 20 twisted-pair cable with a Berg connector on one end only. Available in 25 ft lengths.
d. H856 Berg connector. Includes an H856 Berg connector and 40 pins. Crimping tools are available from: Berg Electronics, Inc., New Cumberland, Pa. 17070.

REGISTERS



The register addresses can be changed by altering the jumpers on the address selection logic. However, any arograms or other software referring to these addresses must also be modified accordingly if the jumpers are changed.

Control and Status Register (DRCSR) 767 770

The control and status register is used to enable interrupt logic and to provide user-defined command and status functions for the external device.

Two REQUEST bits, which are under device control, may be used to provide device status indications, or may be used to initiate interrupts when used with associated INT ENB (interrupt enable) bits which are under program control. Two other bits (CSRO and CSR1) are controlled from the UNIBUS and serve as command bits.

Although the REQUEST and CSR bits can be used for any function the user desires, standard PDP-11 interface conventions attempt to allocate bit 15 for error conditions and bit 7 for ready indications and both of these bits can generate interrupt requests. In addition, bit 0 is normally used for start or go commands.

DRCSR Bit Assignments

BIT	NAME	FUNCTION
15	REQUEST B	This bit is under control of the user's device and may be used to initiate an interrupt sequence or to generate a flag that may be tested by the program. When used as an interrupt request, it is set by the external device and initiates an interrupt provided the INT ENB B bit (bit 05) is also set. When used as a flag, this bit can be read by the program to monitor external device status. When the maintenance cable is used, the state of this bit is dependent on the state of CSR1 (bit 01). This permits checking interface operation by loading a 0 or 1 into CSR1 and then verifying that REQUEST B is the same value. Read-only bit. Cleared by INIT when in Maintenance Mode.
07	REQUEST A	Performs the same function as REQUEST B (bit 15) except that an interrupt is generated only if INT ENB A (bit 06) is also set. When the maintenance cable is used, the state of REQUEST A is identical to that of CSRO (bit 00). Read-only bit. Cleared by INIT when in Maintenance Mode.

06	INT ENB A	Interrupt enable bit. When set, aliows an interrupt sequence to be initiated, provided REQUEST A (bit 07) becomes set. Can be loaded or read by the program (read/write bit). Cleared by INIT.
05	INT ENB B	Interrupt enable bit. When set, allows an interrupt sequence to be initiated, provided REQUEST B (bit 15) becomes set. Can be loaded or read by the program (read/write bit). Cleared by INIT.
01	CSR1	This bit can be loaded or read (under program control) from the UNIBUS and can be used for a user-defined command to the device (appears only on Connector No. 1). When the maintenance cable is used, setting or clearing this bit causes an identical state in bit 15 (REQUEST B). This permits checking operation of bit 15 which cannot be loaded by the program. Read/write bit (can be loaded or read by the program). Cleared by INIT.
00	CSRO	Performs the same functions as CSR1 (bit 01) but appears only on Connector No. 2. When the maintenance cable is used, the state of. this bit controls the state of bit 07 (REQUEST A). Read/write bit. Cleared by INIT.

Output Buffer Register (DROUTBUF) 767 772

The output buffer is a 16-bit read/write register that may be read or loaded from the UNIBUS. Information from the bus is loaded into this register under program control. At the time of loading, a pulsed signal (NEW DATA READY) is generated to inform the user's device that the register has been loaded. The trailing edge of the positive pulse should be used to allow the data to be loaded and settle on the user's input lines. Data from the buffer is transmitted to the user's device on the data OUT lines by means of a DATO or DATOB bus cycle.

The contents of the output buffer register may be read at any time by means of a DATI or DATIP bus cycle. During the read operation, the output of the buffer is fed directly to the bus data lines.

Whenever the maintenance cable is used, the data from the output buffer is also applied to the input buffer register. This permits checking operation of the interface logic.

The DROUTBUF is cleared by INIT.

Input Buffer Register (DRINBUF) 767 774

The input buffer is a 16-bit read-only register that receives data from the user's device for transmission to the UNIBUS. Information to be read is provided by the user's device on the data IN signal lines. Because the input buffer consists of gating logic rather than a flip-flop register, the data IN lines must be held until read onto the bus. The register is read by a DATI sequence and the data is transmitted on the UNIBUS for transfer to the processor or some other device. When the input lines are read during a DATI sequence, a pulsed signal (DATA TRANSMITTED) is sent to the user's device to inform it that the transfer has been completed. The trailing edge of the positive-going pulse indicates that this transfer is completed,

Whenever the maintenance cable is used, the input buffer register receives data from the output buffer register rather than from the user's device. This permits checking of the interface logic by loading a word from the bus into the output register and verifying that the same word appears in the input buffer.

Input and Output Signals

Inputs			outputs		
Signal	Connector	Pin	Signal	Connector	Pin
IN00	2	TT	OUT00	1	C
IN01	2	LL	OUT01	1	K
IN02	2	H	OUT02	1	NN
IN03	2	BB	OUT03	1	U
IN04	2	KK	OUT04	1	L
IN05	2	HH	OUT05	1	N
IN06	2	EE	OUT06	1	R
IN07	2	cc	OUT07	1	T
IN08	2	Z	OUT08	1	W
IN09	2	Y	OUT09	1	X
IN10	2	W	OUT10	1	Z
IN11	2	V	OUT11	1	AA
IN12	2	U	OUT12	1	BB
IN13	2	P	OUT13	1	FF
IN14	2	N	OUT14	1	HH
IN15	2	M	OUT15	1	JJ
REQ A	1	LL	NEW DATA RDY*	1	VV
REQ B	2	S	DATA TRANS.*	2	C
			CSRO	2	K
			CSR1	1	DD
			INIT	1	P
			INIT	2	RR, NN

* Pulse signals, approximately 400-ns wide. Width can be changed by user.

Pin Connections

M971		DR11-C				M971	
		Connector No. 2		Connector No. 1			
Board	Berg Header	Pin	Name	Name	Pin	Berg Header	Board
u2	A	vv	OPEN	OPEN	A	W	Al
U1	B	uu	GND	OPEN	B	uu	A2
V2	C	TT	IN00	OUT00	C	T-r	Al
V1	D	ss	GND	OPEN	D	ss	A2
T2	E	RR	INIT H	OPEN	E	RR	B1
T1	F	PP	GND	OPEN	F	PP	B2
T2	H	NN	INIT H	OPEN	H	NN	C I
T1	J	MM	GND	GND	J	MM	c 2
s2	K	LL	IN01	OUT01	K	LL	D1
S1	L	KK	IN04	OUT04	L	KK	D2
R2	M	JJ	GND	GND	M	JJ	El
R1	N	HH	IN05	OUT05	N	HH	E2
P2	P	FF	OPEN	INIT H	P	FF	F1
P1	R	EE	IN06	OUT06	R	EE	F2
N2	S	DD	GND	GND	S	DD	H1
N1	T	cc	IN07	OUT07	T	cc	H2
M2	U	BB	IN03	OUT03	U	BB	J1
MI	V	AA	GND	GND	V	AA	J2
L2	W	Z	IN08	OUT08	W	Z	K1
L1	X	Y	IN09	OUT09	X	Y	K2
K2	Y	X	GND	GND	Y	X	L1
K1	Z	W	IN10	OUT10	Z	W	L2
J2	AA	V	IN11	OUT11	AA	V	M I
J1	BB	U	IN12	OUT12	BB	U	M2
H2	cc	T	GND	GND	cc	T	N1
H1	DD	S	REQ B	CSR1	DD	S	N2
F2	EE	R	GND	GND	EE	R	P1
F1	FF	P	IN13	OUT13	FF	P	P2
E2	HH	N	IN14	OUT14	HH	N	R1
El	JJ	M	IN15	OUT15	JJ	M	R2
D2	KK	L	GND	GND	KK	L	S1
D1	LL	K	CSRO	REQ A	LL	K	s2
c2	MM	J	GND	GND	MM	J	T1
Cl	NN	H	IN02	OUT02	NN	H	T2
B2	PP	F	OPEN	GND	PP	F	T1
B1	RR	E	IN02	OUT02	RR	E	T2
A2	ss	D	OPEN	GND	ss	D	V1
Al	l-r	C	DATA TRANS.	OPEN	TT	C	v2
A2	UU	B	OPEN	GND	uu	B	U1
Al	VV	A	OPEN	NEW DATA RDY	VV	A	u2

BC11K Connections

Twisted Pair	Color	Pin	Connector No. 1	Connector No. 2
black/white-orange	black	A	OPEN	OPEN
	wh-org	B	OPEN	OPEN
black/white-yellow	black	C	OUT00	DATA TRANS.
	wh-yel	D	OPEN	OPEN
black/white-grey	black	E	OPEN	IN02
	wh-gry	F	OPEN	OPEN
black/white-red	black	H	OPEN	IN02
	wh-red	J	GND	GND
black/white-green	black	K	OUT01	CSRO
	wh-grn	L	OUT04	GND
brown/green	brown	M	GND	IN15
	green	P	INIT	IN13
brown/ red	brown	N	OUT05	IN14
	red	R	OUT06	GND
black/white-blue	black	S	GND	REQ B
	wh-blu	T	0 UT07	GND
black/orange	black	U	OUT03	IN12
	orange	V	GND	IN11
black/white-violet	black	W	OUT08	IN10
	wh-vio	X	OUT09	GND
black/ red	black	Y	GND	IN09
	red	Z	OUT10	IN08
brown/yellow	brown	AA	OUT1 1	GND
	yellow	BB	OUT12	IN03
black/ blue	black	c c	GND	IN07
	blue	DD	CSR1	GND
brown/orange	brown	EE	GND	IN06
	orange	FF	OUT13	OPEN
brown/ blue	brown	HH	OUT14	IN05
	blue	JJ	OUT15	GND
black/yellow	black	KK	GND	IN04
	yellow	LL	REQ A	IN01
brown/violet	brown	MM	GND	GND
	‘violet	NN	GUT02	INIT

black/violet	black	PP	GND	GND
	violet	RR	OUT02	INIT
black/green	black	ss	GND	GND
	green	TT	OPEN	IN00
pink/white-red	pink	uu	GND	GND
	wh-red	vv	NEWDATA RDY	OPEN

SPECIFICATIONS

Usage:	Priority interrupt interface control
Input/output levels: (user interface)	logic 1 = +3 V logic 0 = 0 V
Register Addresses	
Control and Status (DRCSR)	767 770
Output Buffer (DROUTBUF)	767 772
Input Buffer (DRINBUF)	767 774
2nd DR11-C	767 760 to 767 764
3rd DR11-C	767 750 to 767 754
4th DR11-C	(etc) (etc)
UNIBUS Interface	
Interrupt vector addresses:	floating (see Appendix A) (2 needed for each DR1 I-C)
Priority level:	BR5 (may be changed)
Bus loading:	1 bus load
Mechanical	
Mounting:	1 SPC slot
Size:	quad module
Input Current:	1.5A at +5V (no current needed at −15V)

Miscellaneous:

Inputs: One standard TTL unit load; diode protection clamps to ground and +5V

outputs: TTL levels capable of driving 8 unit loads except for the following:

NEW DATA READY = 30 unit loads

DATA TRANSMITTED = 30 unit loads

INIT (initialize) = common signal on both connectors driven by one 30-unit load driver

Signals: NEW DATA READY-drives 30 units, positive pulse, 400-ns wide unless width changed by an external capacitor

DATA TRANSMITTED-drives 30 unit loads, positive pulse, 400-ns wide unless width changed by an external capacitor

INIT (initialize)-common signal on both connectors driven by one 30-unit load driver

Data Inputs: 16-bit word from the external device

Data Outputs: 16-bit word from the UNIBUS. Either a full word or an 8-bit byte (either high or low) may be loaded from the bus.

Maintenance Mode: A MAINT cable (supplied with basic system) jumpers the DROUTBUF outputs to the DRINBUF inputs and forces bits 15 and 7 to read as CSR1 and CSRO, respectively.

Parts List for Interface

Reference Number in Circuit	I.C. Number			Price *
1	SN7404			.70
2	SN7400			.55
3	SN7402			.55
4	SN7402			.55
5	SN7474			.88
6	SN74123			2.40
7	SN74123			2.40
8	SN74193			3.3;
9	SN74164			6.55
10	DM8820			3.09
11	DM8820			3.63
12	DM8830			3.09
13	DM8830			3.09
14	SN74193			3.30
15	SN74152			7.80
16	SN7402			.55
17	SN7400			.55
18	Magnecraft W107-DIP-1 Relay			4.00
Connectors				
J1	DEC H-856			8.00
J2	DEC H-856			8.00
IMP Conn.	Amphenol 48-10R-18-31S			62.00
Resistors	(all 1/4 Watt 5%, $.06 ea.)			
1	39 ohm			.06
8	100 ohm			.48
1	120 ohm			.06
16	180 ohm			.96
3	1K ohm			.18
1	3.3K ohm			.06
1	10K ohm			.06
4	22K ohm			.24
Capacitors				
1	.002 mfd mylar			.30
4	100 pf mica		.25 ea.	1.00
18	.01 mfd. ceramic	.13 ea		2.34
1	5 mfd tantalum			.564
1	10 mfd. tantalum			
Diodes				
2	3.6V .5 Watt zeners	1N5227B	.80 ea.	1.60
19	1N4148		.25 ea.	4.75
Circuit Board				
	Douglass Electronics	ll-DE-11		24.75
			Total	$ 162.26

(excludes labor, connecting wire, solder, etc.)

* 1976 Catalog prices