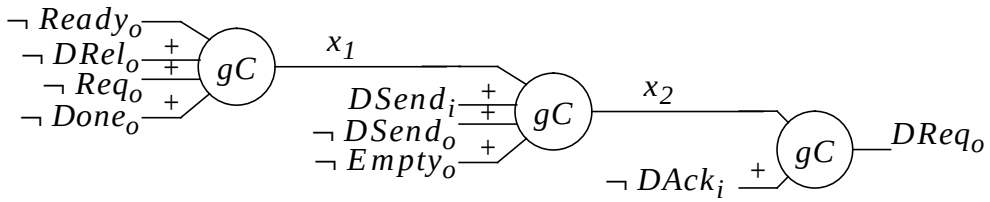


$$\neg\, Ready_o \wedge \neg\, DRel_o \wedge \neg\, Req_o \wedge \neg\, Done_o \rightarrow x_1\uparrow$$
$$Ready_o \rightarrow x_1\downarrow$$
$$DSend_i \wedge \neg\, DSend_o \wedge \neg\, Empty_o \wedge x_1 \rightarrow x_2\uparrow$$
$$\neg\, x_1 \rightarrow x_2\downarrow$$
$$\neg\, DAck_i \wedge x_2 \rightarrow DReq_o\uparrow$$
$$\neg\, x_2 \rightarrow DReq_o\downarrow$$

Figure 7: A speed-independent implementation of the signal $DReq_o$ of the target-send burst-mode cycle of the SCSI data transfer controller.

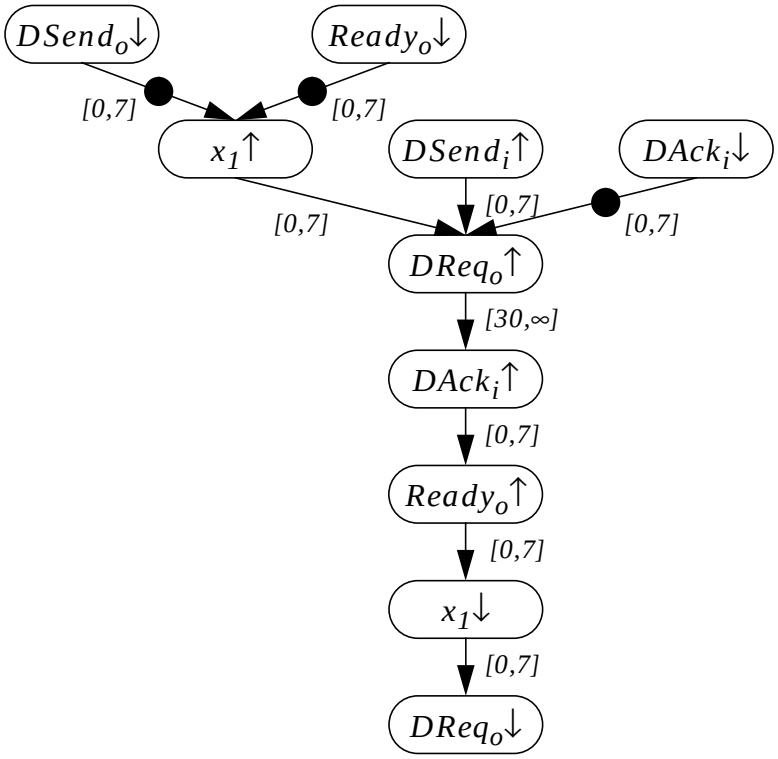


Figure 5: A portion of the cyclic constraint graph for the target-send burst-mode cycle of a SCSI data transfer controller after a successful decomposition.

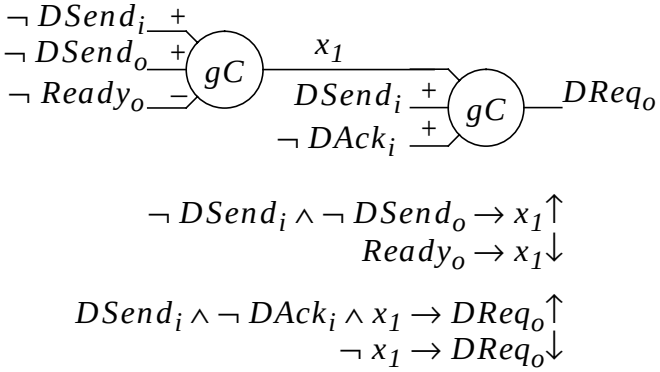


Figure 6: A timed implementation for the signal $DReq_o$ of the target-send burst-mode cycle of the SCSI data transfer controller.

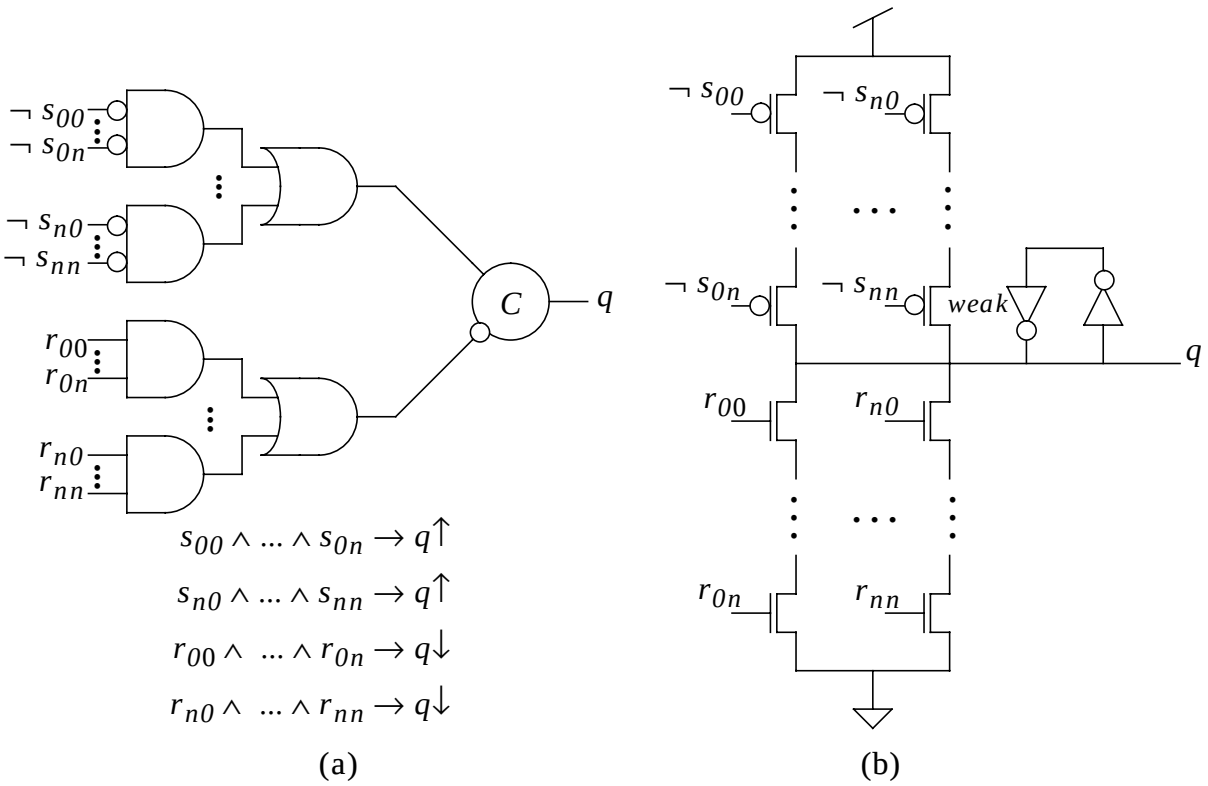


Figure 3: The generalized C-element structure.

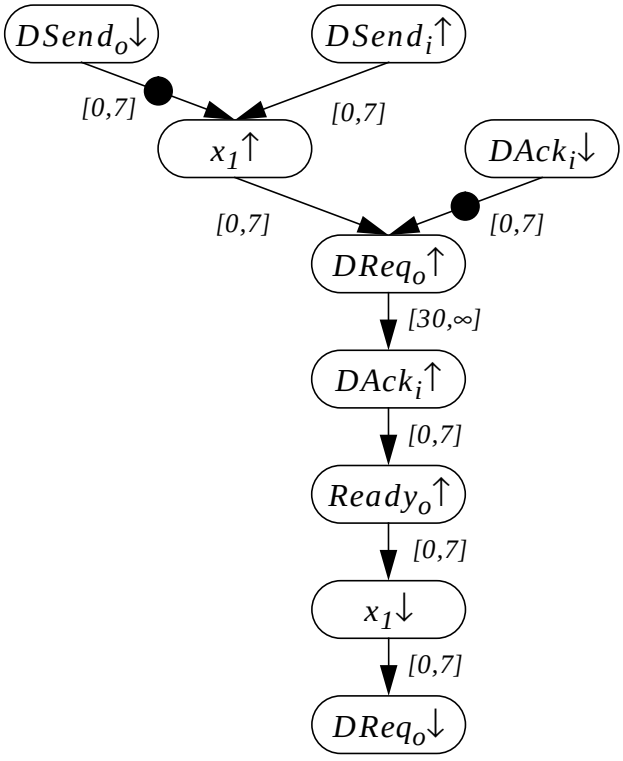
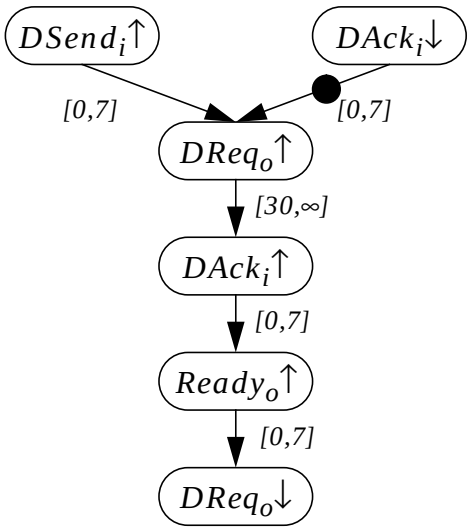


Figure 4: A portion of the cyclic constraint graph for the target-send burst-mode cycle of a SCSI data transfer controller after a decomposition.



(a)

$$DSend_i \wedge \neg DAck_i \wedge \neg DSend_o \wedge \neg Ready_o \wedge \neg DRel_o \wedge \neg Req_o \wedge \neg Done_o \wedge \neg Empty_o \rightarrow DReq_o\uparrow$$
$$Ready_o \rightarrow DReq_o\downarrow$$

(b)

Figure 1: (a)A portion of the cyclic constraint graph for the target-send burst-mode cycle of a SCSI data transfer controller, and (b) production rules for the signal $DReq_o$.

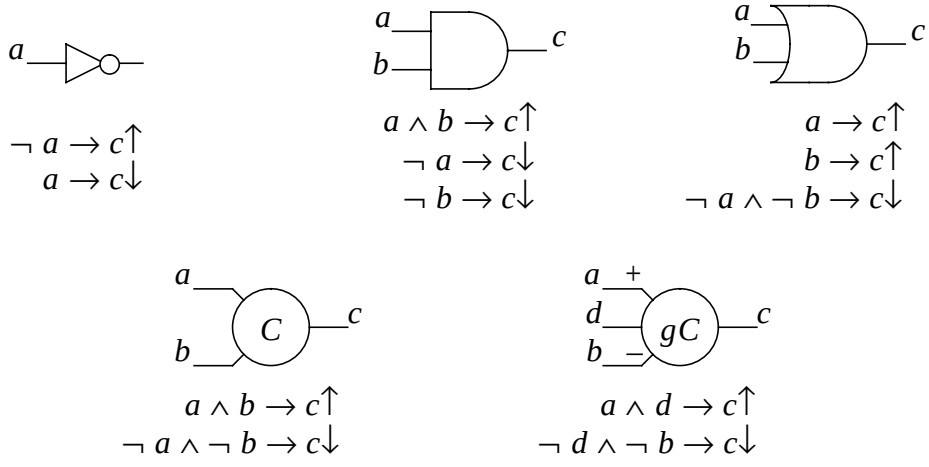


Figure 2: Production rules for several common gates.